DESIGN AND DEVELOPMENT OF 1-D CMUT ARRAY WITH DIAMOND MEMBRANE

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ABSTRACT

DESIGN AND DEVELOPMENT OF 1-D CMUT ARRAY WITH DIAMOND MEMBRANE

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This thesis presents a new microfabrication method of 1-D capacitive micromachined ultrasonic transducer (CMUT) array featuring diamond membrane. This microfabrication method for diamond membrane CMUT array is based on the sacrificial etching of polysilicon in XeF_2 plasma. The stiction problem of membranes due to capillary force in wet etching processes is avoided since the XeF_2 is a gaseous chemical in plasma form that etches silicon and its derivatives with very high selectivity over silicon dioxide and diamond. The developed microfabrication process flow, the realization of the microfabrication process flow in the computer environment, and the design of the 64-element 1-D diamond membrane CMUT array are explained and demonstrated. In this thesis, in addition to the proposed microfabrication, a CMUT array structure named Faraday caged CMUT and a transmit and receive operation are proposed for electrical crosstalk and parasitic capacitance reduction. The finite element method (FEM) modeling of the regular 2-element 1-D CMUT array and the 2-element 1-D Faraday caged CMUT array are performed. The electrical properties and the electrical crosstalk of these CMUT arrays are examined and compared through computational analysis.

Keywords: Capacitive Micromachined Ultrasonic Transducer (CMUT) Arrays, Ultrasound, Microfabrication, Diamond, Crosstalk

ÖZ

ELMAS MEMBRANLI 1-B CMUT DİZİLERİNİN TASARIMI VE GELİŞTİRİLMESİ

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Bu tez çalışmasında elmas membranlı 1-B kapasitif mikroüretilmiş ultrasonik çevirgeç (CMUT) dizisinin mikroüretimi için yeni bir mikroüretim yöntemi sunulmaktadır. Elmas membranlı CMUT dizisi için geliştirilen bu mikroüretim süreci, polisikonun XeF_2 plazması içerisinde feda aşındırmasına dayandırılmıştır. XeF_2, silikon ve türevlerini silikon dioksit ve elmas üzerinde çok yüksek bir seçicilikle aşındıran plazma formunda gaz halinde bir kimyasal olduğundan, ıslak aşındırma işlemlerinde kılcal kuvvet nedeniyle oluşan membranların yapışma sorunu önlenmiştir. Geliştirilen mikroüretim süreci, mikroüretim sürecinin bilgisayar ortamında gerçekleştirilmesi ve elmas membranlı 64 elemanlı 1-B CMUT dizisinin dizaynı anlatılmış ve gösterilmiştir. Bu tez çalışmasında, geliştirilen mikrofabrikasyona ek olarak, elektriksel çapraz etkinin ve parazitik kapasitenin azaltılmasına yönelik, Faraday kafeslenmiş CMUT dizisi olarak adlandırılmış bir CMUT dizi yapısı ve verici ve alıcı operasyonu önerilmiştir. 2 elemanlı 1-B olağan CMUT dizisinin ve 2-elemanlı 1-B Faraday kafeslenmiş CMUT dizisinin sonlu eleman methodu modellemesi gerçekleştirilmiştir. Modellenen CMUT dizilerinin elektriksel özellikleri ve elektriksel çapraz etki bilgisayar ortamında incelenmiş ve karşılaştırılmıştır.

Anahtar Kelimeler: Kapasitif Mikroüretilmiş Ultrasonik Çevirgeç (CMUT) dizileri, Ultrason, Mikroüretim, Elmas, Çapraz etki

To My Beloved Family

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CHAPTER 1

INTRODUCTION

Micro electro-mechanical systems (MEMS) has been categorized as one of the most promising technologies for the 21st century as it is an innovative technology in which silicon-based microelectronics are combined with micromachining technology for both developing and industrial products. The market value of the MEMS reached $11.6 billion in 2018, with consumer applications accounting for more than 60 % of the total market, and it is estimated to have an $18.7 billion market value in 2024 with an increase of 8.3 % annually between 2019-2024 [1].

Capacitive micromachined ultrasonic transducers (CMUTs) generate and receive ultrasonic waves based on the electrostatic force between two electrodes with a gap between them and the motion of the moveable membrane, which also composes one of those two electrodes. The innovations in the microfabrication technology enabled the realization of the first CMUT in the mid-1990s, in which CMUT consisted of a large number of capacitive cells with an operation regime of megahertz [2]. Nowadays, the enhancements in the microfabrication techniques enable the microfabrication of improved CMUTs that are compatible with commercialized piezoelectric transducers and have a substantial potential for medical imaging and treatment applications.

CMUT is a MEMS based device that converts electrical energy to mechanical energy and vice versa [3,4]. CMUTs have become an exciting nominee that capture the attention of many research institutions (Stanford, Fraunhofer, VTT, Leti, Imec), foundries (Philips, Global Foundries, Micralyne, Silex), and companies (Hitachi, Siemens, General Electric, Samsung, Vermon, Kolo, Butterfly) due to their fascinating potential in a wide range of areas such as ultrasonic imaging, therapy,

industrial cleaning, photoacoustic imaging, and air-coupled ultrasonic applications [5,6]. The impedance matching to the fluid environment is better in CMUTs than those piezoelectric transducers because of the low mechanical impedance of a thin membrane. Consequently, CMUTs show a wider operational bandwidth than piezoelectric transducers in immersion, resulting in the removal of the need for a matching layer and improved image resolution [26,27]. Tissue harmonic imaging is achievable due to the broad bandwidth operation of CMUTs. In addition to acoustic benefits, CMUTs offer design flexibility, high sensitivity, long lifetime, low power requirement, wide operating temperature range, CMOS compatible wafer-level microfabrication, and wide frequency operation. Commercial production of CMUTs for medical use demonstrates the capacitive devices' potential against mature piezoelectric counterparts.

1.1 Objective of the Thesis

In this thesis, a new microfabrication method for diamond membrane CMUT array that is based on sacrificial release technique is introduced. Detailed objectives of the thesis are given below:

- Instead of existing microfabrication process flow for diamond membrane CMUT arrays that was based on direct wafer bonding technique and thus showing a yield problem for large CMUT arrays, proposing a new microfabrication process flow for diamond membrane CMUT arrays that is based on surface micromachining technique.
- Microfabrication of 64-element 1-D CMUT array having a conductive diamond membrane and therefore eliminating the requirement for metal top electrode using the new microfabrication process flow which includes:
    - Deposition of Boron-doped nanocrystalline diamond (BNCD) on the processed Silicon-on-Insulator (SOI) wafer using the hot-filament chemical vapor deposition (HFCVD) technique.

    - Sacrificial etching of polysilicon in XeF_2 plasma to release diamond membrane.
    - Deposition of Low temperature oxide (LTO) to achieve vacuum-sealed CMUT cells.
- Designing 64-element CMUT array that operates as a high intensity focused ultrasound (HIFU) array in collapse-snapback mode of operation, and as an Ultrafast (FAST) array in collapse mode of operation.
- Proposed Faraday caged CMUT and a transmit and receive operation to reduce electrical crosstalk and parasitic capacitance.
- Finite Element Method (FEM) modeling of 2-element 1-D CMUT array based on the proposed microfabrication.
- FEM modeling of 2-element 1-D CMUT array based on the Faraday caged CMUT.
- Analysis of the parasitic capacitance and electrical crosstalk of the 2-element 1-D CMUT arrays of Faraday caged CMUT.

CHAPTER 2

CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS

CMUTs were reported as a new type of ultrasonic transducer developed in Ginzton Laboratory of Stanford University in 1994 with high performance and good characterization [3,9,10]. Afterwards, a microfabrication method for integration of CMUT with CMOS technology was proposed [4]. The exciting potential in CMUTs has continued with the studies on developing a theoretical model of CMUT [11].

2.1 CMUT Theory

2.1.1 Equivalent Circuit Model of Circular CMUT Cells

Understanding the equivalent circuit model of CMUT cells and the theoretical background of CMUT cells is essential for designing, analyzing, and optimizing the CMUT. Even though the finite element method (FEM) is a powerful tool for analyzing CMUT devices, this is a computer-intensive technique that might have a high computational cost and might take a very long time [12,13].

The transducers in MEMS technology commonly include both electrical and mechanical components. CMUT is one of the devices that features both electrical and mechanical behavior. The equivalent circuit model of the CMUT cell can be constructed by converting mechanical variables into electrical variables and mechanical components into corresponding circuit components.

The first time an equivalent circuit model for CMUT cell was constructed by converting mechanical components into corresponding electrical components [14]. It was assumed that the CMUT cell would be operated in conventional mode, the top electrode would be the membrane, the membrane motion has piston-like motion, and

the small signal AC would be applied. The circuitry consisted of two parts: the mechanical part and electrical part, in which the circuitry was driven from the electrical part, and the electrical part is connected to mechanical parts through a transformer. The electrical part represents the capacitive behavior of the CMUT cell and consists of a single capacitor, whereas the mechanical part represents the mechanical behavior. The force was defined as across variable and represented by voltage in the circuitry, whereas velocity was defined as through variable and represented by current. Thus, the mass of the membrane was converted into an inductor, and the spring constant of the membrane and the spring softening effect were converted into two different capacitances. The voltage ratio of the transformer was defined as the derivative of the force applied on the membrane due to the electrostatic attraction force to the applied AC signal. It was observed that the developed equivalent circuit mode represents the CMUT cells operating in conventional mode quite well enough.

It has been known that the frequency response of CMUT cells is affected by the operating medium. The effect of the operating medium of the CMUT cell was included in the equivalent circuitry of the CMUT cell [15]. The medium was added as the load to the mechanical part of the circuitry and modeled as mass and damping components. So that, the medium was added to the circuitry as a load consisting of an inductor and a resistance. The developed ANSYS simulation of CMUT cells operating in fluid environment tested the developed equivalent circuitry, including the medium effect.

In the following years, the equivalent circuit model was improved by inserting a more accurate displacement profile of the membrane into the model's equations instead of assuming that it is piston-like motion [16]. Since the movement of the membrane is not constant throughout the membrane, the velocity profile of the membrane is also not constant throughout the membrane. Thus, in the equivalent circuitry, the current variable was defined to represent the average velocity of the membrane. Therefore, in the improved circuit model for the CMUT cell operating in conventional mode, the inductance and the capacitance on the mechanical part of the

circuit were reformulated. Furthermore, the radiation impedance of the medium was defined as a clamped radiator instead, a piston radiator since the displacement profile of the membrane was redefined. Finally, it was observed that the accuracy of the equivalent circuit was improved according to the comparison made with FEM simulations.

A lumped element non-linear circuit model for circular CMUT cell operating in conventional mode was developed in which the current variable is defined to represent the root mean square (RMS) of the velocity over the membrane instead of average velocity [12,13]. A large signal equivalent circuitry was constructed in which, instead of a transformer, dependent sources were used for relating the applied AC voltage to the force on the membrane.

Furthermore, the small signal equivalent circuit model for circular CMUT cell operating in conventional mode was constructed from the lumped element non-linear circuit model, assuming the applied AC signal is small [12,13]. Frequency response of small signal equivalent circuitries of CMUT cell operating in conventional for different current definitions (assuming a constant velocity profile, taking the average of the velocity, and taking the RMS of the velocity throughout the membrane) was calculated. The results were compared with the FEM result of the CMUT cell, and it was observed that the small signal model for the CMUT cell in which the current represents the RMS of the velocity throughout the membrane is the most accurate one.

2.1.1.1 Large Signal Model

In this thesis work, for designing the diamond membrane CMUT array, the lumped element non-linear circuit model [12,13] for circular CMUT cell operating in conventional mode is used. Thus, this circuit model is explained in detail in this part. The lumped element non-linear circuit model for circular CMUT cell operating in conventional mode is given in Figure 2.1 [12,13].

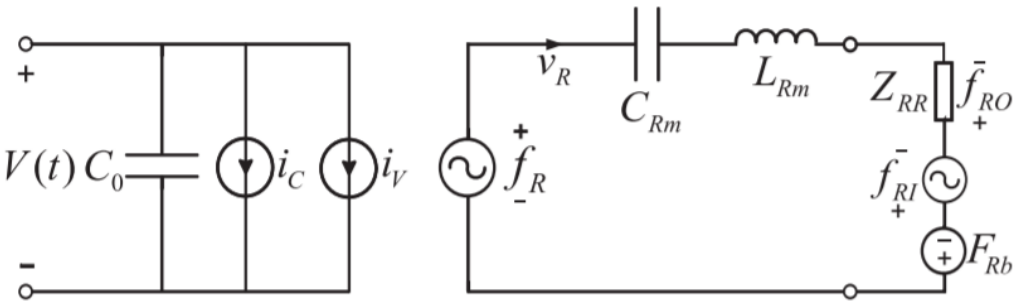


Figure 2.1. Lumped element non-linear circuit model for circular CMUT cell operating in conventional mode [12,13].

The parameters found in Figure 2.1 which are C_0, i_C, i_V, f_R, C_{Rm}, L_{Rm}, Z_{RR}, f_{RI}, F_{Rb} symbolized the total capacitance of the CMUT cell when no voltage is applied, the capacitance current, the velocity current, applied force on the membrane, the compliance of the membrane, the mass of the membrane, the radiation impedance of the medium, the acoustic pressure applied by the medium on the membrane, and the force applied by the medium on the membrane, respectively.

According to the developed equivalent circuit model for large signal model parameters given in the circuit model (Fig. 2.1) were formalized as in the following equations (Eq. 2.1-2.5) [12,13]

$$i_C(t) = C(t)\frac{\partial V(t)}{\partial t} - C_0\frac{dV(t)}{dt} = \left(C_0\, g\left(\frac{x_p(t)}{t_{ge}}\right) - C_0\right)\frac{dV}{dt} \tag{2.1}$$

$$i_V(t) = \frac{2f_R(t)}{V(t)}v_R(t) = \sqrt{5}\,\frac{C_0V^2(t)}{t_{ge}}\,g'\left(\frac{x_p(t)}{t_{ge}}\right)v_R(t) \tag{2.2}$$

$$C_{Rm} = 1.8\,\frac{(1-\nu^2)a^2}{16\pi E{t_m}^3} \tag{2.3}$$

$$L_{Rm} = \rho_m t_m \pi a^2 \tag{2.4}$$

$$f_R(t) = \frac{\partial E(t)}{\partial x_R} = \sqrt{5}\frac{\partial E(t)}{\partial x_P} = \sqrt{5}\,\frac{C_0V^2(t)}{2t_{ge}}\,g'\left(\frac{x_p(t)}{t_{ge}}\right) \tag{2.5}$$

Where t_{mem},, r_{mem}, ν¸ E, ρ_m, t_{ge} and $x_p(t)$ are the thickness and radius of membrane, poison's ratio, Young's modulus, and density of the membrane material, the effective

gap height, and peak displacement, respectively. C_0 is the total capacitance of the CMUT at zero bias and is equaled to $\varepsilon_0 2\pi r_{mem} \mathrm{d}r/t_{ge}$. The function g(.) and g'(.) were defined as

$$g(u) = \frac{\tanh^{-1}(\sqrt{u})}{\sqrt{u}} \tag{2.6}$$

$$g'(u) = \frac{1}{2u}\left(\frac{1}{1-u} - g(u)\right) \tag{2.7}$$

The radiation impedance of the medium, $Z_{RR,}$ was given as

$$Z_{RR} = \pi\rho_0 c\left(1 - \frac{20}{(ka)^9}[F_1(2ka) + jF_2(2ka)]\right) \tag{2.8}$$

where ρ_0 is the density, and c is the speed of sound of the operating medium and $F_1(y) = (y^4 - 91y^2 + 504)J_1(y) + 14y(y^2 - 18)J_0(y) - \cdots$

$$y^5/16 - y^7/768 \tag{2.9}$$

$$F_2(y) = -(y^4 - 91y^2 + 504)H_1(y) + 14y(y^2 - 18)H_0(y) - \cdots$$

$$y^5/16 - y^7/768 \tag{2.10}$$

J_n and H_n are the nth order Bessel and Struve functions, respectively.

For the collapse voltage quantification, the static behavior of the circuitry given in Figure 2.1 was considered. The peak displacement of the membrane at collapse and the collapse voltage were formulized as in the following equations (Eq. 2.11-2.12)

$$X_{P,col} \approx t_{ge}\left(0.4648 + 0.5433\frac{F_{Pb}}{F_{Pg}} - 0.01256\left(\frac{F_{Pb}}{F_{Pg}} - 0.35\right)^2 - 0.002775\left(\frac{F_{Pb}}{F_{Pg}}\right)^9\right) \tag{2.11}$$

$$V_{col} = V_r\left(0.9961 - 1.0468\frac{F_{Pb}}{F_{Pg}} + 0.06972\left(\frac{F_{Pb}}{F_{Pg}} - 0.25\right)^2 + 0.01148\left(\frac{F_{Pb}}{F_{Pg}}\right)^9\right) \tag{2.12}$$

where F_{Pb} is the external static force, in other words deflection, F_{Pg} is the maximum external static force to deflect membrane until collapse that is equal to $t_{ge}/5C_{Rm}$.

2.1.1.2 Small Signal Model

The small signal equivalent circuit model derived from the large signal model in which the AC signal was assumed to be small compared to the applied DC voltage. The small signal equivalent circuit for circular CMUT cell operating in conventional mode is given in Figure 2.2 [12,13].

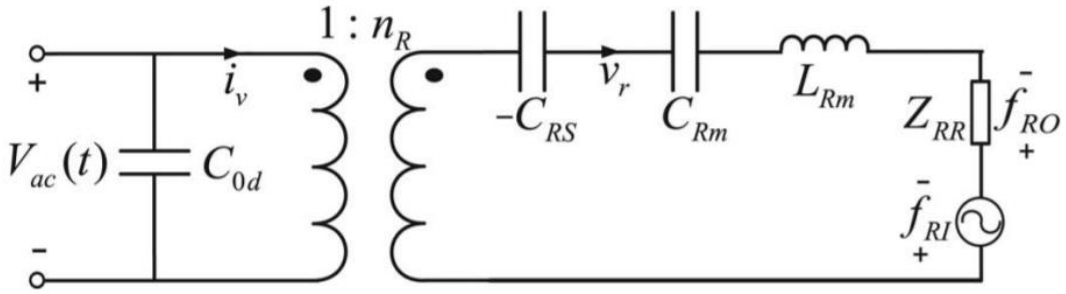


Figure 2.2. The small signal equivalent circuit for circular CMUT cell operating in conventional mode [12,13].

According to the developed equivalent circuit model for large signal model parameters given in the circuit model (Fig. 2.1) were formalized as in the following equations (Eq. 2.13-2.14) [12,13]

$$\eta_R = \frac{2F_R}{V_{DC}} \tag{2.13}$$

$$C_{RS} = \frac{2t_{ge}^2}{5C_0V_{DC}^2 g''(X_P/t_{ge})} \tag{2.14}$$

where the term F_R is the rms value of the static force on the membrane with the applied DC bias and the function g''(.) were expressed as

$$F_R = \sqrt{5}\,\frac{C_0V_{DC}^2}{2t_{ge}}\,g'\left(\frac{X_P}{t_{ge}}\right) \tag{2.15}$$

$$g''(u) = \frac{1}{2u}\left(\frac{1}{(1-u)^2} - 3g'(u)\right) \tag{2.16}$$

and the term X_P is the static peak displacement of the membrane with the applied DC bias.

The developed equivalent circuit model is useful for calculating the frequency response of the CMUT cell. However, to formulate the resonance frequency of a single CMUT cell in immersion, some other publications in the literature were searched for.

Based on the given small signal circuitry of circular CMUT cell, for a medium with a negligible radiation impedance, such as air, the resonance frequency of the CMUT cell can be expressed as in the following equations [17,18]

$$f_{0,vacuum} = \frac{w_0}{2\pi} = \frac{1}{2\pi\sqrt{L_{Rm}\left(\frac{1}{C_{Rm}} - \frac{1}{C_{RS}}\right)^{-1}}} \tag{2.17}$$

$$f_{0,vacuum} = \frac{2.95 \times t_{mem}}{2\pi \times {r_{mem}}^2}\sqrt{\frac{E}{\rho_m(1-\nu^2)}} \tag{2.18}$$

The resonance frequency of a CMUT cell in immersion, in which the radiation impedance of the medium is effective, was approximated as follows [19]

$$f_{0,medium} = \frac{f_{0,vacuum}}{\sqrt{1+0.67\times\frac{\rho_0 \times r_{mem}}{\rho_m \times t_{mem}}}}$$

(2.19)

Furthermore, the collapse voltage in these publications [17-19] were expressed as

$$V_{collapse}|_{P_{atm}=0} = \frac{1.56}{{r_{mem}}^2}\sqrt{\frac{E\times {t_{mem}}^3 \times {d_{eff}}^3}{\varepsilon_0 \times(1-\nu^2)}} \tag{2.20}$$

that is approximated to the collapse voltage formulation given in Eq. 2.12 and can be used for modeling of a single CMUT cell other.

2.1.2 CMUT Mode of Operations

Conventional, collapse, and collapse-snapback modes of the CMUT can be used for transmit and receive operations [3,4,20,21]. The conventional mode is the first used operational mode in the CMUT history. In this mode, CMUTs are operated at a DC

bias voltage lower than the collapse voltage of the membrane so that there is still a gap between the membrane and the bottom electrode. Due to electrostatic attraction, when a DC bias is applied between two electrodes, the top electrode (membrane) moves towards the bottom electrode. The membrane would vibrate and generate acoustic waves when AC voltage is applied between the electrodes. The membrane's vibration magnitude increases with the applied DC bias resulting in higher power transmission.

Furthermore, when there is an incoming acoustic wave, the membrane movement would generate AC detection currents due to a change in the capacitance. The change in the capacitance would be greater for higher DC bias, resulting in improved sensitivity. Thus, in conventional mode, it is advantageous to operate the CMUT as possible as close to collapse voltage [22]. On the other hand, the total applied voltage, the sum of applied DC bias and AC signal, should pass the collapse voltage, resulting in a trade-off between efficiency and acoustic output pressure. In Figure 2.3, the conventional mode of operation of a CMUT is shown.

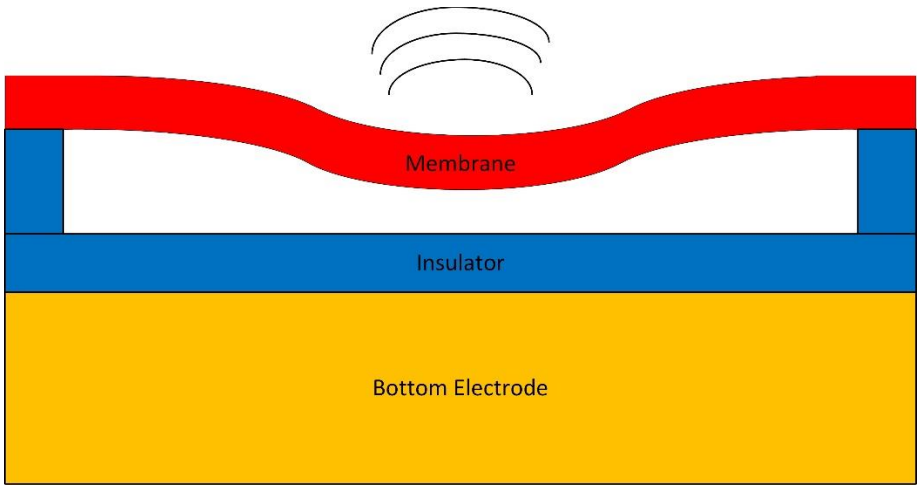


Figure 2.3. The conventional mode of operation of a CMUT

The collapse mode was examined for the first time in 2003 at Stanford University [23]. In this mode, first, a DC bias voltage higher than the collapse voltage is applied to collapse the membrane on the bottom electrode. Second, the bias voltage is reduced to a value between the collapse and the snapback voltages without releasing

the membrane. Third, the CMUT is excited with an AC voltage, keeping the total applied voltage between collapse and snapback voltages. In this mode of operation, the center of the membrane is in touch with the bottom electrode throughout the operation. It is shown that CMUT has higher coupling efficiency, which influences the power transmission, sensitivity, and image resolution, in the collapse mode of operation than it has in the conventional mode of operation [24]. Furthermore, since a lesser area of membrane is vibrating in collapse mode, the resonance frequency of the membrane decreases approximately to its half in this mode operation. The decrease in the resonance frequency can be controlled by the applied DC voltage. In Figure 2.4, the collapse mode of operation of CMUT is shown.

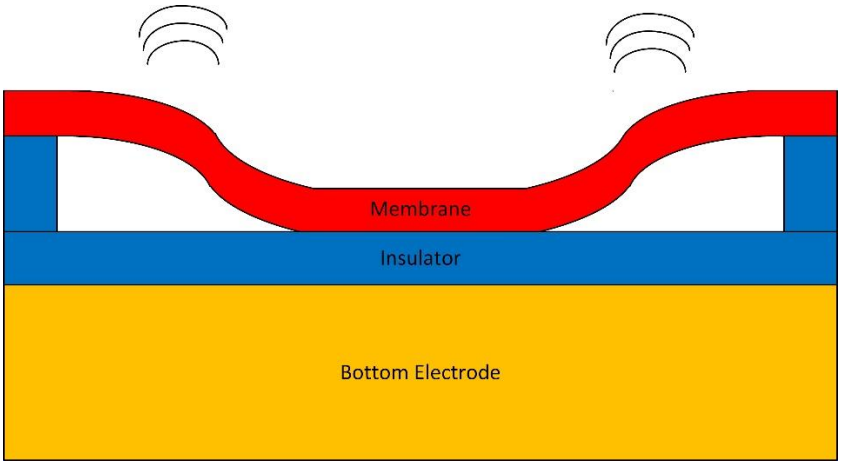


Figure 2.4. The collapse mode of operation of CMUT.

The collapse-snapback mode of CMUT was observed for the first time in 2005 at Stanford University [25]. In this mode, the membrane is collapsed onto the bottom electrode in the collapse cycle as it is collapsed in the collapse mode of operation. However, different from the collapse mode, in this operational mode, the membrane is released during the snapback cycle to achieve a more extensive range of deflection of the membrane. The essential aim of this operation is to provide higher power output. This is achieved by providing a larger deflection of the membrane [25]. In Figure 2.5, the collapse-snapback mode of operation of CMUT is shown.

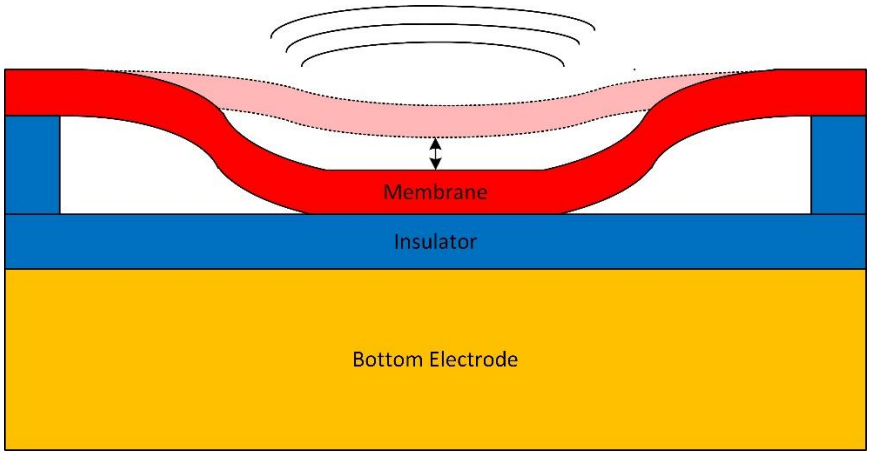


Figure 2.5. The collapse-snapback operation of CMUT.

2.2 CMUT Microfabrication Techniques

It is reasonable to categorize CMUT processes according to the hottest process step throughout the microfabrication if there is an electronic integration since the temperature influences [26]. Therefore, it is essential not to exceed 400°C if there is an electronic integration during a process step. Such processes are categorized as low-temperature processes and can be referred to as CMOS compatible, whereas others are named as high-temperature processes, and it is not possible to integrate those with electronics during the microfabrication. The processes based on the wafer bonding technique, especially those including fusion bonding, are a good example of a high-temperature process and not compatible with post-processing on CMOS chips. On the other hand, processes based on sacrificial release can be either low-temperature or high-temperature processes.

There are two main process techniques widely used in CMUT microfabrication: wafer bonding and sacrificial release.

2.2.1 Wafer Bonding Technique

In the microfabrication of CMUTs, wafer bonding is a widely used and preferable technique that includes surface microfabrication and silicon on insulator (SOI) technologies. This technique significantly simplifies the fabrication and results in finer uniformity and control [27].

In the wafer bonding technique, there are three basic technologies: anodic, fusion, and adhesive bonding [26]. In those wafer bonding technologies, fusion bonding of silicon comes a step forward, and it is used in many MEMS microfabrications. This technique requires high temperature and clean surface of bonding faces. Furthermore, the stability and enabling fabrication of complex structures such as membranes from single-crystal silicon, a well-known, studied, and characterized material, make this technology interesting.

In Figure 2.6 process flow of the typical microfabrication of CMUT device featuring silicon membrane based on wafer bonding technique is given [27]. The process starts with heavily doping of Si-wafer (Fig. 2.6.a). This is essential since this layer will be the bottom electrode of the CMUT and thus required to be highly conductive. Then, the process continues with thermal oxidation of the prime wafer to define the gap height (Fig. 2.6.b). This step is followed by featuring the thermally grown oxide by lithography and reactive ion etching to define the shape and dimension of the CMUT cavity (Fig. 2.6.c). After that, second thermal oxidation is performed to define the insulation layer of the CMUT (Fig. 2.6.d). The quality of the second thermal oxide is essential to prevent hysteresis during the device operation due to trap of charges during ion drift and to prevent dielectric breakdown, which might result in failure of the device operation. At this point, it might be beneficial to flatten the surface and get rid of any bumps that occurred around the CMUT cavities due to the famous phenomenon called bird's peak to increase the success probability of wafer bonding. Then the bonding of the processed primary wafer and an SOI wafer is performed in which the device layer of the SOI wafer will define the membrane, and thus the thickness and the conductivity of the device layer should be arranged accordingly.

In the bonding, the oxidized Si wafer is in contact with the silicon face of the device layer of the SOI wafer (Fig. 2.6.e.). The following step is releasing of the handle and buried oxide (BOX) layer to form the CMUT membrane in which the handle wafer is removed using mechanical grinding. A wet etchant of silicon such as KOH or tetramethylammonium hydroxide (TMAH) might be used to remove the remaining silicon in which the BOX layer would be the etch stop. Then the BOX layer is removed by hydrofluoric acid (HF) or by a derivative of HF such as buffered HF (BHF), in which the device layer Si is used as the etch stop (Fig. 2.6.f). At this point of the process, the CMUT, including the bottom electrode, membrane, anchor, and isolation layer is constructed. From now on, the required contact to the top electrode and bottom electrode and the isolation of the CMUT array elements is constructed. For this purpose, etching via through the Si wafer is constructed to form the required topside contact to the bottom electrode (Fig. 2.6.g). Then, the metal sputtering is performed to provide the required contacts (Fig. 2.6.h). Finally, metal featuring is performed to separate metal pads from each other and isolate CMUT array elements (Fig. 2.6.i).

This technique offers improved control over the membrane thickness, gap height, and less residual stress in the membrane [27]. Furthermore, this technique enables the microfabrication of piston CMUT and post-CMUT, in which the membrane thickness or the CMUT structure is arranged so that the membrane displacement behavior is closer to the behavior of a piston membrane. On the other hand, the main disadvantage of this technique is the wafer bonding step itself since this step requires as clean surfaces as possible, low surface roughness, and even may result in low yield of bonding performance. Another drawback of this technique might be the cost and the complexity of obtaining proper SOI wafers.

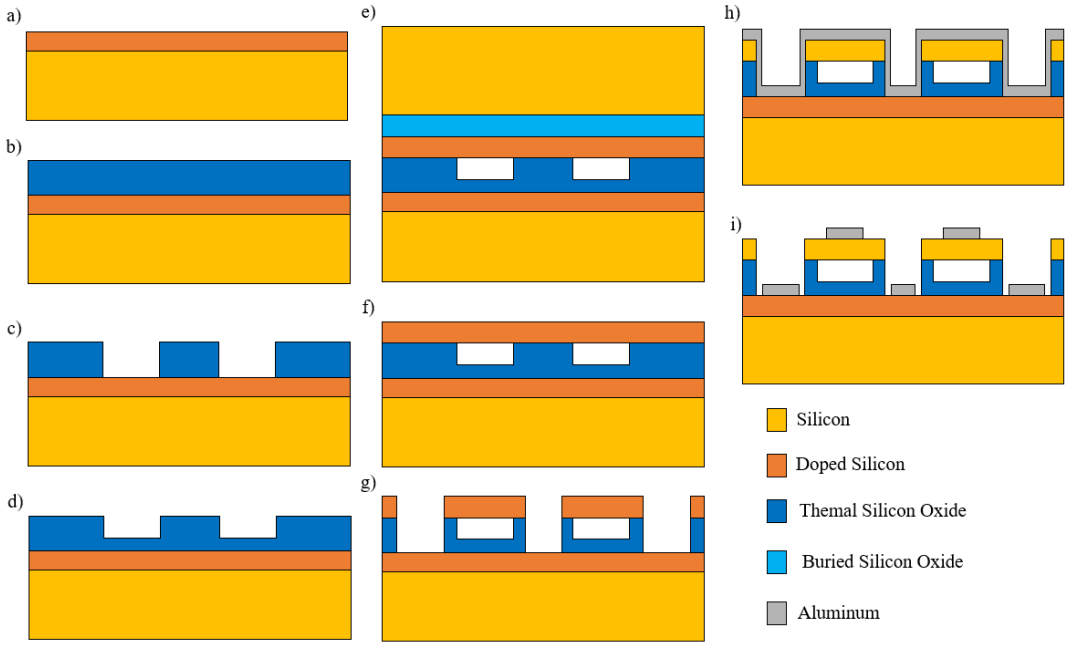


Figure 2.6. Process flow of the typical microfabrication of CMUT device featuring silicon membrane based on wafer bonding technique [27]. (a) Top side highly doped starting prime wafer. (b) First thermal oxidation. (c) Etch to form cavity. (d) Second thermal oxidation. (e) Wafer bonding of prime and SOI wafers. (f) Removal of handle wafer and buried oxide. (g) Etching through Si wafer. (h) Metal sputtering. (i) Metal patterning and device isolation.

2.2.2 Sacrificial Release Technique

The first process developed for the microfabrication of CMUT is based on the sacrificial release technique [26,27]. This type of process is classified as surface micromachining process in which the gap of the CMUT cell is constructed by sacrificial etching of sacrificial layer (that is placed between the membrane and the substrate) through the etch hole and etch channel. The vacuum-sealing of the CMUT gap is realized by sealing deposition, in which oxide or nitride is deposited at low pressure, and seal the gap by filling the etch channel.

The membrane uniformity is one of the essential concerns for the sacrificial release processes since the deposition uniformity might not be as desired and thus result in

different device performance through the wafer. Another important topic for this process is the control over the height and thickness of the gap and membrane and insulation layer since these parameters have an important impact on device characteristics and might result in unexpected or undesired device performance.

Furthermore, membrane stress is another issue in the sacrificial release process where one should be careful about membrane having compressive stress since it would result in buckling up of the membrane and affect the device performance adversely. Thus, the material selection for isolation, sacrificial and membrane layers, and the release agent is important since those have an essential role in the above concerns. The release agent's selectivity should be as high as possible since it is intended to remove the sacrificial layer, whereas the structural layers (insulation and membrane) would be conserved during the sacrificial etching. The various material selection for the sacrificial release processes is given in Table 2.1. [10,26,28-32]

Another solution was developed in 2003 by Siemens and patented in which polysilicon is used as both the sacrificial and membrane layer. For this purpose, it was proposed to use thin silicon nitride as a protective layer for polysilicon membrane during the sacrificial release [33].

Stiction is a universal problem with all wet release processes, which arises from the capillary forces during the drying process following the wet release and might result in stiction of the structural layer (membrane) to the substrate accordingly to the stiffness of the structural layer. However, there are some solutions to overcome this problem, such as freeze-drying [34], supercritical drying [35], and dry release [36-38]. A more efficient way to overcome this stiction problem is using a dry release process in which, different from the wet release process, a gaseous chemical in plasma form removes the sacrificial layer instead of a wet chemical [26]. For a silicon dioxide or diamond membrane, removing silicon or polysilicon sacrificial layer in XeF_2 plasma is an example of a dry release process.

Table 2.1. Various material selection for sacrificial release based CMUT microfabrication [10,26,28-32].

Insulation Layer	Sacrificial Layer	Membrane Layer	Release Agent	Selectivity	Notes
LPCVD Si_3N_4	LPCVD Poly-Si	LPCVD Si_3N_4	KOH	Very good	-
LPCVD Si_3N_4	LPCVD LTO	LPCVD Poly-Si	HF	Excellent	High membrane stress
LPCVD Si_3N_4	LPCVD LTO	LPCVD Si_3N_4	HF	Poor	Non-uniform membrane
PECVD Si_3N_4	PECVD LTO	PECVD Si_3N_4	HF	Poor	Non-uniform membrane, high membrane stress
PECVD Si_3N_4	Polymide	PECVD Si_3N_4	H_2SO_4 + H_2O_2	Excellent	Limited gap height control

For the sealing of the CMUT cavities, LPCVD silicon nitride deposition is one of the techniques that is used widely. The conformal deposition of LPCVD silicon nitride, which means equal deposition in the vertical and lateral direction, is an advantageous feature. LPCVD nitride sealing is preferable, especially when the etch hole is small (defined by E-beam lithography) since it is deposited almost equally in the vertical and lateral dimension of the etch hole and thus seal the hole from the top [39,40]. LPCVD silicon nitride has a low sticking coefficient, and thus, molecules can go through the etch channel without sticking. This might be problematic since it might result in the deposition of silicon nitride inside the cell cavity. Long and labyrinth shape etch channels might be helpful to solve this problem. Also, it is preferable to choose the height of the etch channel less than the height of the cavity to lessen sealing deposition inside the cavity [39,40]. Another solution is using a sealing material with a higher sticking coefficient, such as low temperature oxide

(LTO). So that more molecules would be stuck to the etch channel walls and trapped inside the etch channel, and thus, less of them would be able to go inside the cavity.

In Figure 2.7 process flow of the typical microfabrication of CMUT device featuring silicon nitride membrane based on sacrificial release technique is given [27]. The material selection is as in the first column in Table 2.1 since this selection is preferable to others with any important drawbacks. The process starts with heavily doping of Si-wafer. This is essential since this layer will be the bottom electrode of the CMUT and thus required to be highly conductive. Then, the process continues with the silicon nitride deposition, the insulation layer, which also conserves the Si substrate from being etched during the sacrificial release, followed by deposition of the first polysilicon layer. After that, polysilicon is patterned by lithography and RIE to define the etch channel area (Fig. 2.7.a). Following that, a second polysilicon deposition is performed to construct the etch channels placed nearby the CMUT cells (Fig. 2.7.b). After that, silicon nitride deposition is realized to form the membrane layer (Fig. 2.7.c), followed by patterning the silicon nitride by lithography and RIE to define the etch holes (Fig. 2.7.d). The next step is the sacrificial release of the silicon nitride membrane. For this purpose, potassium hydroxide (KOH) solution is used to remove the polysilicon where silicon nitride and silicon nitride covered Si substrate is not etched noticeably (Fig. 2.7.e). Following the sacrificial release, the sealing of the cavity at low pressure is realized by LPCVD silicon nitride deposition (Fig. 2.7.f). This deposition seals the cavity by filling the thin etch channels. The cavity of the CMUT cell is effectively vacuum-sealed since the deposition is realized at low pressures. Lastly, metallization is realized. For this purpose, Aluminum is deposited on the top side of the wafer and then patterned to define the top electrode and the required metal contacts to the bottom and top electrode (Fig. 2.7.g).

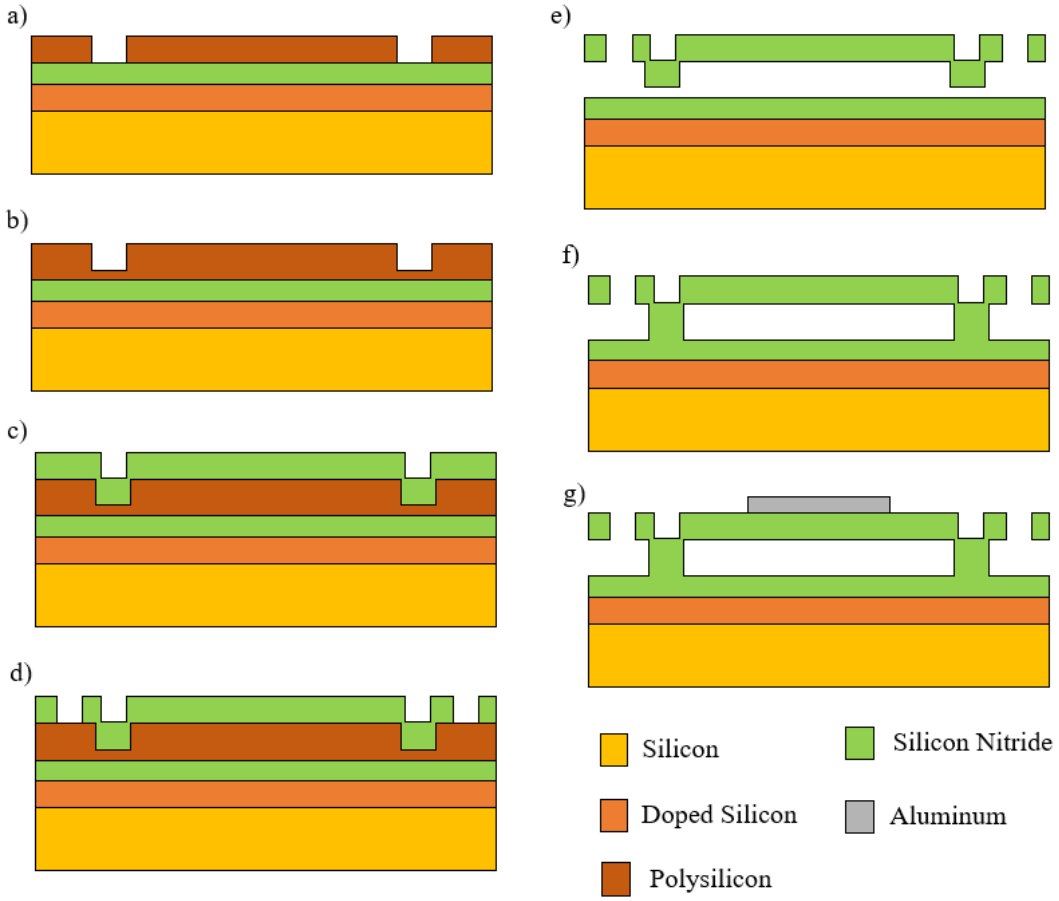


Figure 2.7. Process flow of the typical microfabrication of CMUT device featuring silicon nitride membrane based on sacrificial release technique [27]. (a) Doping of Si wafer, silicon nitride deposition, the first polysilicon layer deposition followed by patterning of the polysilicon. (b) The second polysilicon deposition. (c) Silicon nitride deposition to construct the membrane layer. (d) Patterning of silicon nitride to define etch holes. (e) Sacrificial release of polysilicon in KOH solution. (f) Sealing of the CMUT cavities by LPCVD silicon nitride deposition. (g) Metal deposition and patterning.

The gap height of the CMUT in the given process flow is determined by the combined thickness of the two polysilicon depositions (Fig.2.9.a) and (Fig.2.9.b), whereas the membrane thickness is determined by the combined thickness of two silicon nitride depositions (Fig.2.9.c) and (Fig.2.9.f) [27]. It might be challenging to realize a uniform deposition and thus height and thickness of the gap and membrane.

In addition, the membrane material might have intrinsic stress due to deposition and sacrificial release process steps, altering the device's performance and operation. On the other hand, the process flow is simple and easy to follow. Furthermore, since this process includes only surface microfabrication techniques, it can be classified as reliable. Also, it is possible to design sacrificial release processes with a low maximum processing temperature to allow post-process CMOS and BiCMOS integration. Another essential advantage is that the yield issues faced in the wafer bonding microfabrication are not faced in the sacrificial release microfabrication, enabling the fabrication of large CMUT arrays.

2.3 Diamond Films in MEMS and CMUTs

2.3.1 Diamond as a Material in MEMS

Diamond is a semiconductor material with extreme mechanical properties that make it an attractive material for MEMS. It is one of the materials with a very high Young's modulus to density ratio, which is beneficial in MEMS since this ratio increases the probability of obtaining quasistatic mechanical response that improves the SNR (signal to noise ratio) of the MEMS device [41]. The electrical properties of diamond are also exciting. The resistivity of diamond films can be controlled for an extensive range with Boron (p-type) and Phosphorus (n-type) doping [42]. Furthermore, diamond films are advantageous in terms of high operation frequency, high output power, high thermal conductivity, and thus less heating among the other semiconductors. In addition, diamond is an inert material used in a MEMS device without being oxidized over the years. Another advantage of the diamond is being biocompatible so that it is available to be used in medical devices. CMUTs featuring diamond membrane were microfabricated using the wafer bonding technique [43-51].

The Ashby method is a well-known technique in MEMS devices to choose the optimum material [52]. According to this method, choosing a structural material with high fracture stress and low density is important to reduce shock-induced fracture. In addition to low density, high fracture strength is also required. In Figure 2.8(a), it is given that diamond is one of the materials that show high fracture strength and have low density [52].

Another concern for the Ashby method is the ratio of material's Young's modulus to density [52]. MEMS structures are susceptible to failure by shock-induced stiction. This might occur when adjacent structures are forced into mechanical contact. For this purpose, it is beneficial to choose a material with low density to decrease the magnitude of the inertial load. In addition, to minimize the structural deflection, it would be preferable to choose a material with high Young's modulus. Finally, to increase the probability of obtaining a quasi-static mechanical response, a material having a high square root of the ratio of Young's modulus to density should be chosen. In Figure 2.8(b), it is given that diamond is one of the materials that show a high Young's modulus to density ratio [52].

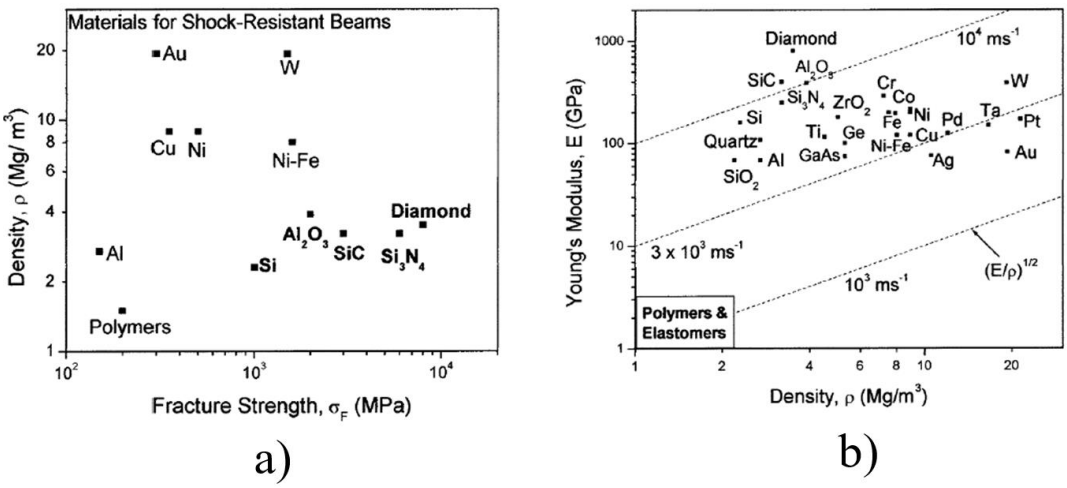


Figure 2.8. The density versus fracture strength (a) and Young's modulus versus density (b) graphs of several materials used commonly in MEMS structures [52].

Having a structural material with a high Young's modulus is desirable since in many MEMS structures, the operating frequency increases with the Young's modulus and decreases with size. Since there is a minimal size limitation due to the technology, with higher Young's modulus, devices with higher operating frequency can be built. Therefore, there is a broader operating frequency band for the structure. The mechanical properties of some widely used membrane materials and diamond is given in Table 2.2 [46,53,54].

Table 2.2. Mechanical properties of some widely used materials [46,53,54].

Parameter	Silicon	Silicon Nitride	Silicon Carbide	Silicon Dioxide	Diamond
Density (kg/m^3)	2332	3270	3210	2200	3520
Young's Modulus (GPa)	160	320	450	73	1200
Poisson ratio	0.29	0.26	0.35	0.17	0.2
Shear Modulus (GPa)	80	65	149	31	577
Hardness (GPa)	10	15.8	32	7.9	100
Thermal Conductivity (W/m.K)	151	30	490	1.3	2200
Fracture Toughness ($MPa.m^{-1/2}$)	1	6.3	5.2	0.7	5.3

During high power transmission and HIFU operation of CMUTs, the membrane might be warm-up since a very high power is generated, and some of that power would transform to heat. In this type of situation, the operation duration of the CMUT device is limited by the thermal conductivity coefficient of the membrane material. If membrane material has a high thermal conductivity coefficient, then the heat generated will be dissipated, and thus, the device will be warm-up slower, and the

operation duration would be longer. Diamond is an extraordinary material with a very high thermal conductivity coefficient, and thus, an interesting membrane material for HIFU CMUTs.

Diamond is advantageous over many other semiconductors in terms of having a high operation frequency, high output power, high thermal conductivity (less self-heating), high breakdown electric field, and no RF current slump. Thus, it is a preferable material for RF operations. Diamond transistor with H-termination (p-type doping) at the surface was microfabricated [55]. The motive behind developing diamond transistors is the expectation to exhibit the best performance in high-power and high-frequency operations. In Figure 2.9, the output power versus operational frequency of some useful semiconductors is given [55]. As observed, diamond has significant potential in terms of high power and frequency operations.

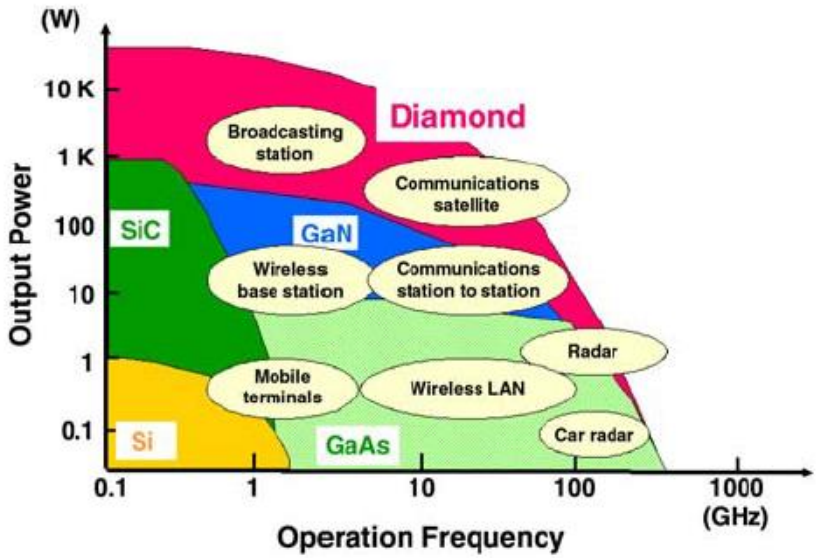


Figure 2.9. Output power versus operational frequency of some semiconductors [55].

In another publication, the diamond transistor was used since diamond transistors should benefit from a high breakdown electric field, high thermal conductivity, low dielectric constant, and high bulk carrier mobility [56]. It was stated that such material properties could lead to high performance in terms of high power

transmission and low loss or high power and high-frequency electronics. As a result, the gate to drain length was increased to improve the breakdown voltage. The highest breakdown voltage of 1530 V for a diamond FET was reported to date. The electrical properties of some widely used semiconductor materials and diamond is given in Table 2.3 [53,57-61].

Table 2.3. Electrical properties of some widely used semiconductors materials [53,57-61].

Parameter	Germanium	Silicon	Silicon Carbide	Gallium Arsenide	Diamond
Dielectric Constant	16.2	11.7	9.66	13.1	5.7
Electrical Resistivity (Ω.cm)	47	$2.3x10^{5}$	10^{9}	10^{8}	10^{16}
Hole Mobility (cm^{2}/V.s)	1900	475	320	400	3800
Electron mobility (cm^{2}/V.s)	3900	1500	800	8500	4500
Breakdown Voltage ($x10^{5}$ V/cm)	1	37	30	4	100
Bandgap (eV)	0.66	1.12	3	1.42	5.5

In nature, diamond is found as a perfect insulator with a very high electrical resistivity. Single crystalline diamond (SCD) and natural diamond films cannot be doped [61]. This is not a desirable property since the conductivity of these films cannot be controlled, and these films are high resistive. On the other hand, other diamond films such as microcrystalline diamond (MCD), nanocrystalline diamond (NCD), and ultrananocrystalline diamond (UNCD) can be doped with boron (p-type) and phosphorus (n-type). It was observed that the resistivity of diamond films could be reduced to 0.001 ohm.cm with proper boron doping. In Figure 2.10, the resistivity of a diamond film versus the boron concentration is given [61]. Another observed

property is that the bandgap of diamond films can be reduced to 0.6 eV with proper phosphorus doping. Thus, it was observed that one could control the resistivity and bandgap of the diamond film with proper boron and phosphorus doping for a very large range.

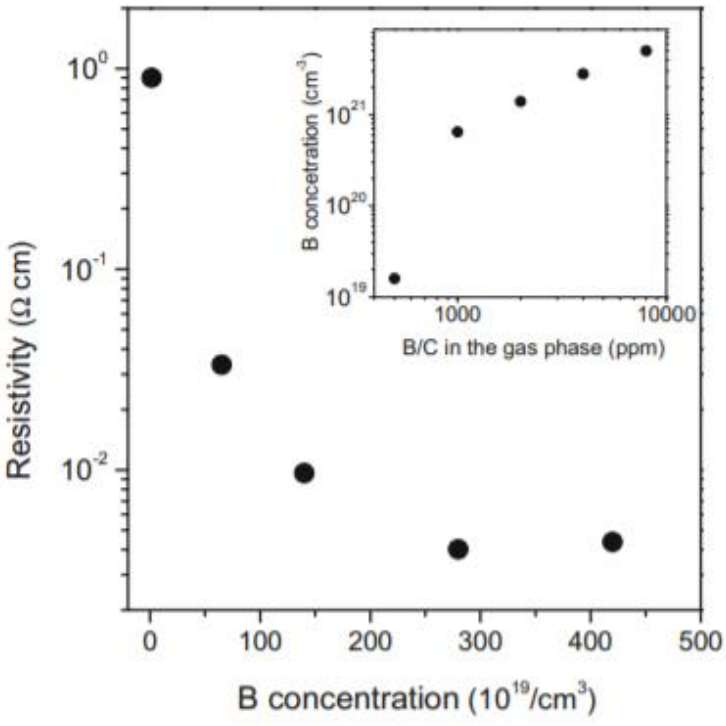


Figure 2.10. The resistivity of a diamond film versus the boron concentration [81].

Natural diamond can be found nearby volcanos. It can be carried to the surface by volcanic eruptions or mining since it is formed under the earth under high temperatures and pressure. For microfabrications containing diamond, synthetic diamond films can be used and deposited on the wafer. Microwave plasma chemical vapor deposition (MPCVD) and hot filament chemical vapor deposition (HFCVD) are two methods used for diamond deposition. The main difference between these deposition methods is the technique used to activate the chemicals. MPCVD uses microwave energy for activation, whereas HFCVD uses hot filaments. Since by MPCVD only a limited part of the wafer can be deposited, to coat a whole wafer, HFCVD is required.

First, the carbon crystal seeding at the surface of the wafer is realized. Afterwards, the diamond is grown on the wafer by introducing a gaseous mixture with a certain recipe into the furnace. The typical gas mixture used for diamond deposition is 1 % CH_4 in H_2. The main growth species in a standard diamond deposition is the CH_3 radical, which adds carbon atoms to the surface following hydrogen absorption by H atoms. In addition to CH_3 radicals, a high concentration of H atoms at the surface is required for diamond deposition [62]. Another gas mixture that is used for diamond deposition includes Ar to the existing CH_4/H_2 mixture so that using $Ar/CH_4/H_2$ gas mixture enables the deposition of UNCD [63]. The ratio of those molecules determines the deposition receipt. The grain size of the deposited diamond film depends on the deposition receipt, where this determines the kind of diamond film: MCD, NCD or UNCD.

The grain size and surface roughness values of diamond films were examined [64]. In Table 2.4 the grain size and the surface roughness values of MCD, NCD and UNCD are given [64].

Table 2.4. Grain size and surface roughness values of diamond films [64].

Parameter	MCD	NCD	UNCD
Grain size (nm)	500-1000	50-100	2-5
Surface roughness (nm)	400-1000	50-100	20-40

Having a high surface roughness and grain size is not desirable since it might end up with high compressive residual stress and poor intergranular adhesion. Thus, MCD films are not as preferable as NCD and UNCD films. From Table 2.4, it is observed that UNCD is the most convenient material for wafer bonding since it has the lowest surface roughness among the others.

Another important issue about diamond films is their material properties. Since the deposition recipe is different for MCD, NCD, and UNCD, the sp^3 covalent bond ratio over the sp^2 covalent bond in the structure might change. This affects the mechanical

and electrical properties of the diamond film. In Table 2.5 comparison of the mechanical and electrical properties of diamond films and the natural diamond itself is given [60,61,65-67].

Table 2.5. Mechanical and electrical properties of diamond films and diamond [60,61,65-67].

Parameter	MCD	UNCD	NCD	Diamond
Density (kg/m^3)	3520	3300	3440	3520
Young's Modulus (GPa)	1120	850	1015	1200
Poisson ratio	0.09	0.07	0.12	0.2
Shear Modulus (GPa)	515	220	450	577
Hardness (GPa)	98	68	86	100
Thermal Conduction Coefficient (W/m-K)	1400	12	1000	2200
Electrical Resistance (Ω-cm)	10^{13}-10^{16} Can be doped	10^{3}-10^{4} Can be doped	10^{13}-10^{16} Can be doped	10^{16}
Dielectric Constant	5.7	3.8	5.6	5.7
Fracture Toughness ($MPa\text{-}m^{-1/2}$)	6.5	3.7	5.6	5

2.3.2 Diamond Membrane CMUT

In the past years, diamond has been an attractive candidate for silicon as a membrane material of CMUTs because of its superior thermal, mechanical, and electrical properties. For developing a similar microfabrication process to the traditional silicon membrane CMUT microfabrication process (which contains direct bonding of SOI wafer to the patterned SiO_2) firstly, the potential of bonding of diamond on insulator (DOI) wafer to the SiO_2 was examined [43]. For this purpose, direct bonding of DOI wafer employing UNCD to thermal silicon dioxide was examined

following some cleaning procedures. It was concluded that deposition of SiO_2 on top of the diamond wafer before bonding is necessary for chemical affinity and successful bonding. A further statement was that the quality (annealing) of the deposited SiO_2 improves the bonding performance.

Following this work, the bonding performance of the DOI wafer employing UNCD to the patterned SiO_2, in which the DOI wafer was coated with PECVD oxide, was examined [44]. The SiO_2 was patterned to construct the cavities for CMUT. It was observed that diamond membranes, including SiO_2, suffer from compressive stress.

Vacuum sealed cavities with NCD and UNCD membranes were microfabricated and characterized [45]. In this microfabrication, instead of PECVD oxide used in previous publications [43,44], diamond wafers were coated with hot temperature oxide (HTO) at 850 °C without burning the diamond film. HTO was chosen since it is more thermally stable and robust compared to PECVD oxide. It was stated that the bonding was successful, and the membrane deflection profile was coherent with the FEM results. It was explained that NCD would be a better choice than UNCD since NCD membranes showed less residual stress, and NCD is a thermally more robust material for HTO deposition.

Microfabrication process flow for UNCD membrane CMUT based on wafer bonding technique was developed [46,47,51,52]. The microfabrication process flow of the diamond membrane CMUT based on the wafer bonding technique is given in Figure 2.11 [46]. The process starts with doping of the prime Si wafer with phosphorus (Fig. 2.11.a). Then, the thermal oxide is grown (Fig. 2.11.b), followed by patterning SiO_2 by lithography and RIE to define the CMUT cavities (Fig. 2.11.c). Thus, the prime wafer is ready for wafer bonding. The top wafer of the bonding pair is UNCD coated Si wafer. HTO is deposited on the top wafer. Following the oxide deposition, chemical mechanical polishing (CMP) is performed in order to decrease the surface roughness for a successful direct bonding (Fig. 2.11.d). Now, both prime and top wafers are ready for wafer bonding.

The next step is plasma-activated direct bonding of the wafers (Fig. 2.11.e). Afterwards, the bulk silicon of the top wafer is removed by grinding and TMAH. SiO_2 is a commonly used hard mask material for diamond patterning in O_2 plasma. For this purpose, PECVD SiO_2 is deposited on top of the UNCD layer (Fig. 2.11.f). The next step is the patterning of SiO_2 hard mask by lithography and RIE followed by patterning of UNCD and then removal of SiO_2 hard mask while patterning of SiO_2 underlying UNCD (Fig. 2.11.g). In this step, Silicon and UNCD act as etch stop for SiO_2 RIE, whereas SiO_2 acts as etch stop for diamond RIE. After that, Al is sputtered for metallization (Fig. 2.11.h). Finally, Al is patterned by lithography and wet etch to construct the top electrode on the membrane and required metal contacts for the bottom and top electrode (Fig. 2.11.i). Since UNCD is not doped and has a resistivity between 10^3-10^4 Ohm.cm, a metal top electrode for the CMUT cell is required.

HTO deposition on the diamond is costly and risky due to high temperature process (Diamond might burn during high temperature processes that include oxide). Also, to provide electrical isolation for the bottom electrode of CMUT array elements, wafer bonding of a device layer patterned SOI wafer with patterned thermal oxide on top on it and the diamond wafer with PECVD SiO_2 coated on it was realized [49].

Microfabrication of CMUT featuring diamond membrane based on wafer bonding technique requires extra smooth surfaces (R_a<0.5nm), as possible as to be free of any particle contaminant and chemical affinity (Si&SiO_2) for successful direct wafer bonding. These constraints lower the yield of bonding and disable the microfabrication of particularly large CMUT arrays having a large number of array elements.

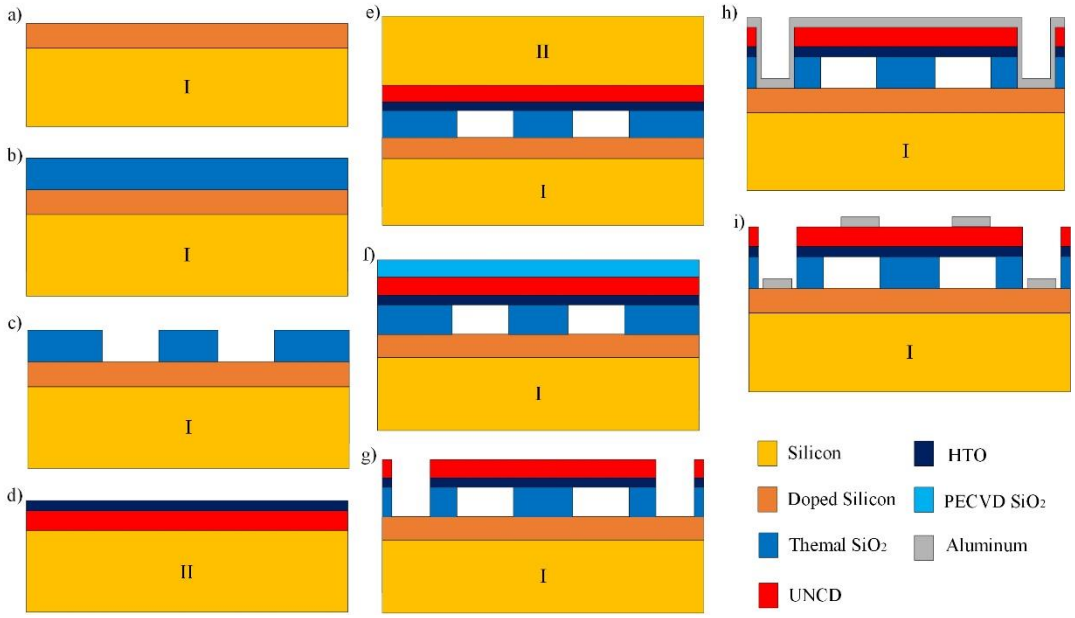


Figure 2.11. The microfabrication process flow of the diamond membrane CMUT based on wafer bonding technique [66]. (a) Top side highly doped starting prime wafer. (b) Thermal oxidation. (c) Patterning of oxide to form cavity. (d) HTO deposition on diamond coated wafer. (e) Wafer bonding of prime and UNCD wafers. (f) Removal of handle wafer, PECVD SiO_2 deposition. (g) Patterning of SiO_2/UNCD/SiO_2. (h) Sputtering Aluminum. (i) Metal patterning.

CHAPTER 3

DESIGN AND MICROFABRICATION OF CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCER FEATURING DIAMOND MEMBRANE

In this chapter, the determination of the CMUT cell size parameters is explained. Then the developed microfabrication for diamond membrane CMUT array is described. The microfabrication is based on sacrificial release of polysilicon in XeF_2 plasma where the CMUT cavities are vacuum-sealed by LTO sealing deposition. The layout design for two identical 64-element 1-D CMUT arrays is realized. The virtual microfabrication of the CMUT array is demonstrated. The virtual analysis of the developed microfabrication is provided.

3.1 Determination of CMUT Cell Parameters

In this study, it was aimed to design a dual array where it operates as a HIFU array in collapse snapback mode and as a FAST array for ultrafast imaging in collapse mode. In general, the resonance frequency of a CMUT cell in collapse mode is around 4 times higher than the collapse snapback mode. Also, generally the HIFU applications are realized for frequency range of 1 to 3 MHz whereas the ultrafast imaging applications are realized for frequencies higher than 6 MHz. Therefore, it was determined to design a CMUT cell that has a resonance frequency at 2 MHz and 8 MHz in collapse-snapback and collapse modes in immersion, respectively.

According to the applied DC bias, in collapse mode the resonance frequency is 2 to 2.5 times higher than it is in conventional mode whereas in collapse snapback mode resonance frequency drops by 1.5 to 2 times compared to conventional mode [7,23-25]. Therefore, considering the aimed resonance frequencies in collapse and collapse snapback modes, it was determined to design a CMUT cell that has a resonance frequency between 3 to 4 MHz in immersion.

The CMUT arrays were designed to be driven by Verasonics Vantage System (Verasonics, USA), which can drive an ultrasound probe up to 100 V. Thus, considering high AC pulse in HIFU operation, a collapse voltage around 70 V was aimed.

Using the equation set, Eq. 2.16-20, for various membrane radius and thicknesses, the resonance frequency under air and water and the required total gap height to match the collapse voltage of 70 V (considering air deflection) were calculated as given in Table 3.1.

Table 3.1. The resonance frequency and the required total gap for various membrane radius and thicknesses, providing the required resonance frequency (between 3-4 MHz in immersion in conventional mode) and collapse voltage (70 V) conditions.

Mem. Thic. (nm), t_m	Radius (μm), r_m	Eff. gap (nm), t_{eff}	Gap (nm), $t_{g,Patm=0}$	Air Def. (nm)	Total gap (nm), t_g	Freq. air (MHz), $f_{0,air}$	Freq water (MHz), $f_{0,water}$
300	13	266	239	20	259	14.61	4.65
	14	293	267	27	294	12.60	3.88
350	15	275	250	22	272	12.80	4.10
	16	300	274	29	303	11.25	3.50
400	16	263	237	19	256	12.86	4.24
	17	285	259	25	284	11.39	3.66
	18	307	282	31	311	10.16	3.18
450	17	253	227	17	244	12.82	4.33
	18	273	248	22	260	11.43	3.77
	19	294	268	27	295	10.26	3.30
500	18	246	220	16	236	12.70	4.39
	19	264	239	20	259	11.40	3.84
	20	282	257	24	281	10.29	3.39

The air deflection of the membrane due atmospheric pressure was calculated through air deflection algorithm developed by ULTRAMEMS Research Group and enabled for public use. The air deflection was considered during the calculation of the required total gap height. During the calculations, a 100 nm thick thermal oxide was considered as the insulation layer.

Considering a feasible CMUT microfabrication, it is beneficial to choose the gap height as high as possible since from the above table it can be seen that gap height will be in terms of nanometers. It would be harder to realize a uniform deposition when the thicknesses are getting lower. This is valid for membrane thickness too, since it is not feasible to realize a uniform diamond deposition at lower deposition amounts.

In addition, there is an etch channel in the CMUT which should have a smaller height compared to gap height as mentioned above. Therefore, it was observed that the most feasible choice would be a 400 nm membrane thickness and 18 μm cell radius, where the total gap height was determined as 300 nm which is a close and rounded number found in Table 3.1. The etch channel thickness was determined to be half of the gap height. Otherwise, as it will be explained in the process flow in detail, one of the sacrificial layers, one for etch channel and one for additional CMUT cavity gap would have a deposition thickness less than 150 nm which would might be problem for uniform deposition for any of those layers.

According to determined values of the cell features, using the resonance frequency and collapse voltage equations (Eq. 2.16-2.20) and the air deflection algorithm the resonance frequency in air and water and the collapse voltage of a single CMUT cell were calculated as 10.16 MHz, 3.18 MHz and 65.62 V, respectively.

Further calculation for a single CMUT cell were performed through the equivalent circuit model found in the literature (Eq. 2.1-2.15). The frequency response of the single CMUT cell for different applied DC bias, the peak displacement versus the applied DC bias and the collapse voltage of the single CMUT cell including the loading effect of the medium were calculated through this model. For this purpose,

a MATLAB script based on these equations of the equivalent circuit model was constructed. The peak displacement versus applied DC voltage of a single CMUT cell (considering the air deflection) was calculated. It was observed that the peak displacement at zero biasing that corresponds to the air deflection, is 30 nm. This is the same value found through the air deflector algorithm. According to the calculated static characteristic of the membrane, the collapse voltage was found as 67.60 V whereas the peak displacement at this collapse was calculated as167.91 nm.

In the small signal model, even though the circuitry is linear, the radiation impedance changes with the operation frequency. Therefore, the radiation impedance was defined as a matrix that depends on the frequency. A frequency set starting from 1 MHz to 7.5 MHz with a step size of 0.1 MHz defined and the small signal velocity of single CMUT cell was solved for each frequency. The small signal velocity of the membrane under 30 V, 40 V, and 50 V DC bias and 1 V AC from 1 MHz to 7.5 MHz is given in Figure 3.1. It is be observed that the resonance frequency of the membrane sweeps from 3.17 to 2.88 MHz, decreasing with the applied bias voltage as expected.

Further calculation of the frequency response of same single CMUT cell in air with were performed for small signal model with a frequency range of 5 MHz to 15 MHz. Small signal response in air was calculated under 30 V, 40 V, and 50 V DC and 1 V AC as depicted in Figure 3.2. As expected, the resonance frequency and the peak velocity was increased in air compared to in immersion.

For a large CMUT array the response may alter compared to the calculated response of a single CMUT cell. The bandwidth of the array is expected to be higher compared to the response of a single CMUT cell. On the other hand, these calculations provided an insight about the behavior and were utilized while designing the CMUT that realizes the mentioned constraints.

CMUTs are beneficial with adjustable resonance frequency with the applied DC voltage. As seen in the Figure 3.1 and 3.2, the resonance frequency of the membrane decreases with the increasing DC bias due to spring softening effect [14]. So any

variation in the resonance frequency due to alteration in the layer thicknesses during the microfabrication can be handled with the applied DC bias.

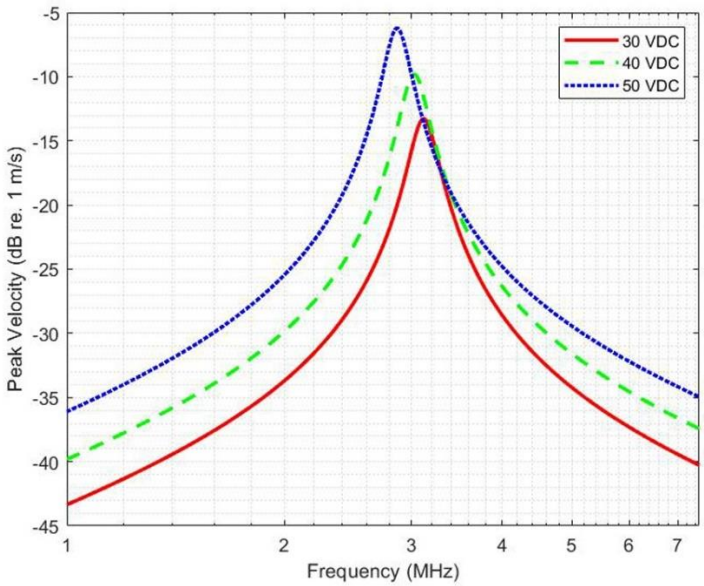


Figure 3.1. The calculated small signal peak velocity of the membrane in immersion under 30 V, 40 V, and 50 V DC bias from 1 MHz to 7.5 MHz.

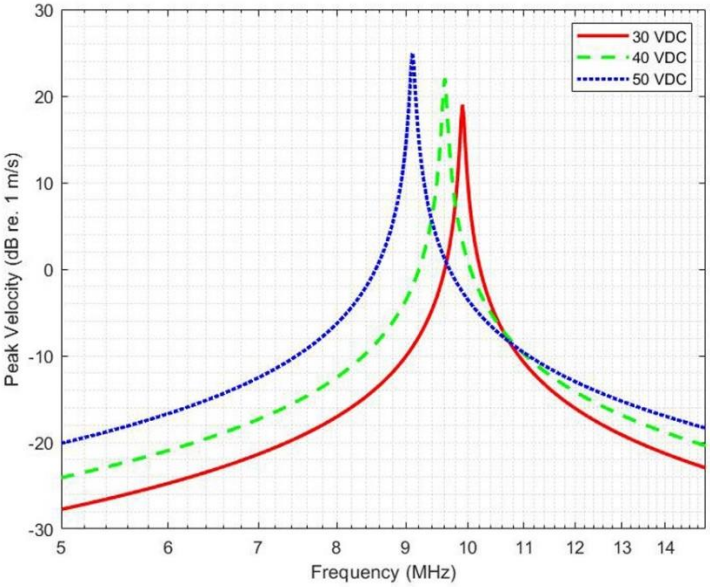


Figure 3.2. The calculated small signal peak velocity of the membrane in air under 30 V, 40 V, and 50 V DC bias from 5 MHz to 15 MHz.

3.2 Developed Microfabrication for Diamond Membrane CMUT Array

In this part, a new microfabrication process flow for diamond membrane CMUT array is introduced. The developed microfabrication process is named as "ULTRAMEMS Sacrificial Release Microfabrication". The process is based on the on the surface microfabrication technique and sacrificial etching of polysilicon in XeF_2 plasma. The microfabrication is determined to be realized on SOI wafer.

"ULTRAMEMS Sacrificial Release Microfabrication" process requires 6 lithography masks and 7 lithography processes steps in total. In the microfabrication, there are 2 polysilicon layers, where both of them are sacrificial layers, 2 thermal oxide layers where both of them are structural, 2 LTO (Low Temperature Oxide) layers where one of them is hard mask and the other one is for sealing, one highly boron doped NCD (BNCD) layer which is the membrane of the CMUT and finally one layer of Tri-Metal (30 nm Ti + 20 nm Cu, 500 nm Au) which is for providing the electrical connections.

3.2.1 Process Flow

"ULTRAMEMS Sacrificial Release Microfabrication" is a microfabrication process flow that is developed to realize microfabrication of BNCD membrane CMUT array. The microfabrication is realized on a SOI wafer. 6 lithography masks are required for this developed microfabrication, where 7 lithography processes exist throughout the microfabrication process flow. Sacrificial polysilicon is chemically dry-etched in XeF_2 plasma where, BNCD, and silicon dioxide layers and the top side of the SOI wafer that is enclosed with thermal oxide are structural layers of the microfabrication.

The process begins with microfabrication of the 6-in SOI wafer. It has n-type doped (5 Ω.cm, P, 450 μm) handle wafer with highly conductive surface (0.005 Ω.cm),

silicon dioxide box layer (1 μm) and highly n-type doped (0.005 Ω.cm, P, 2 μm) device layer (Fig. 3.3).

A highly conductive handle wafer would result in waviness and stress on the wafer due to damage on the crystal structure of the silicon. Also, having a high conductivity at the surface of the handle wafer is sufficient to provide the required grounding of the wafer that carries CMUT arrays and electrical isolation for the CMUT array. Therefore, during the microfabrication of the SOI wafer, ion is implemented on the bonding surface of the handle wafer and then with thermal drive in at 1050 °C for one hour and conductive (0.005 Ω.cm, As) surface is provided. The details about the ion implementation and thermal drive-in and modeling of the process step is provided in the following parts. Some of the highly conductive silicon at the surface turns into silicon dioxide during the thermal oxidation of the handle wafer leaving an approximate depth of 1 μm as highly conductive surface which is sufficient for our grounding purposes.

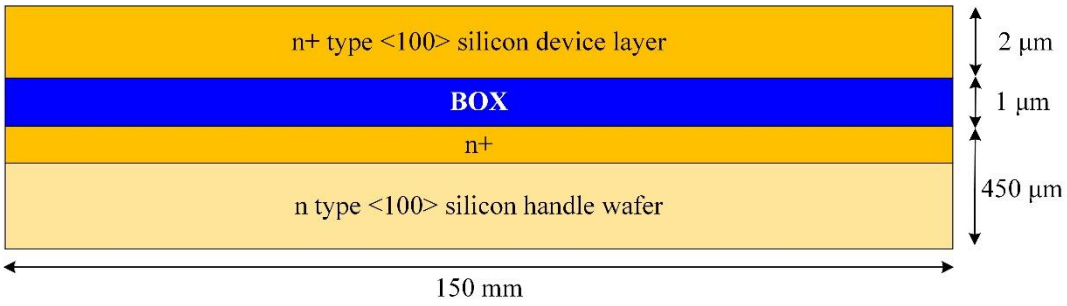


Figure 3.3. 6-in Silicon on Insulator (SOI) wafer that has handle wafer (450 μm, n-type (5 Ω.cm, As)), box layer (1 μm, thermal dioxide) and device layer (2 μm, highly n-type (0.005 Ω.cm, As, <100>).

After the microfabrication of the SOI wafer with specific features, the process flow continues with the patterning of the device layer of the SOI wafer by lithography and RIE (SF_6) (Fig. 3.4). The device layer will be used as a bottom electrode of the CMUT device, and thus isolation between bottom electrodes of different array elements must be provided. Since the aspect ratio is low due to low the thickness of the device layer (2 μm) and high width of the trench (>20 μm), RIE would be enough.

“BottomElectrode-Mask#1” mask is used during the exposure of the photoresist while the lithography type is light.

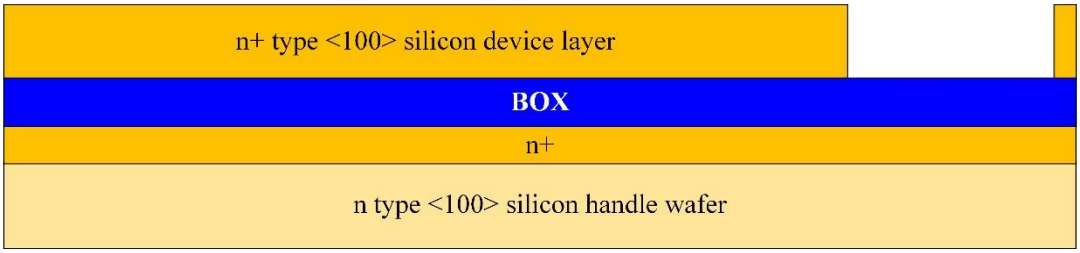


Figure 3.4. Patterning of the device layer of the SOI wafer with lithography and RIE (SF_6) for bottom electrode definition..

Patterning of the device layer of the SOI wafer is followed by first thermal oxide growth (THEROX1) (Fig 3.5). Including the following process steps, the final thickness of this layer is aimed to be 250 nm at the end of the microfabrication. The thickness of this layer would be affected by another thermal oxidation process step where the insulation layer is constructed. The thermal oxide insulation layer thickness is determined to be 100 nm, which would be sufficient enough for CMUT device to operate up to 100 V DC bias [68]. The determination of the final thickness of the THEROX1 layer is based on the cavity gap, etch channel height and isolation layer thickness. As mentioned, the thickness of the insulation layer is planned to be 100 nm whereas the difference between the final thicknesses of THEROX1 and insulation layer must be equal to the difference between the cavity gap and etch channel height. Therefore, a final thickness of 250 nm is aimed for THEROX1 layer and considering the following thermal oxidation, 220 nm thermal oxide is growth in this process step. Therefore, in the following thermal oxidation process step, the thickness of the thermal oxide should be increased by 30 nm.

The receipt of this thermal oxidation step is as follows; start with 30 minutes of dry oxidation, then wet oxidation and a final 30 minutes of dry oxidation (dry (30 min)/wet/dry (30 min)). Here the thickness of the thermally grown oxide is mainly determined by the wet thermal oxidation, whereas the first and the last dry oxidations are for increasing the quality of the thermal oxide. The effect of the first and the last

dry oxidations on thickness should be considered, since 220 nm oxide is growth in this process step which is a considerably a thin thermal oxide layer.

In the thermal oxidation algorithm developed by ULTRAMEMS Research Laboratory that is opened for public use, one can observe the realistic growth thickness. According to this algorithm at 1000° C after the first 30 minutes of dry oxidation, 30.5 nm oxide would be growth. After that, with 23 minutes of wet oxidation, the total oxide thickness would be 211.8 nm. Finally, with another 30 minutes of dry oxidation, the final oxide thickness would be 219.7 nm that was the aimed thickness for THEROX1 layer. Since the thermal oxide thickness is insignificant compared to device layer thickness the alteration of the device layer thickness can be neglected.

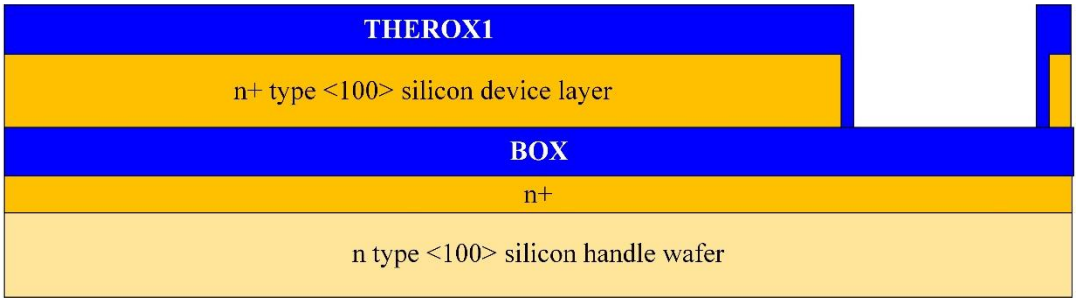


Figure 3.5. Thermal growth (220 nm) of the first thermal oxide layer (THEROX1) by dry (30 min)/wet/dry (30 min) oxidation.

Thermal oxidation is followed by patterning of the THEROX1 layer by lithography and RIE (CHF_3 + CF_4) (Fig. 3.6). The goal of this process step is to etch thermal oxide inside of the active area and thus define the active area of CMUT cells. Silicon will be the etch stop for oxide patterning. “ActiveArea-Mask#2” mask is used during the exposure of the photoresist, while lithography type is dark.

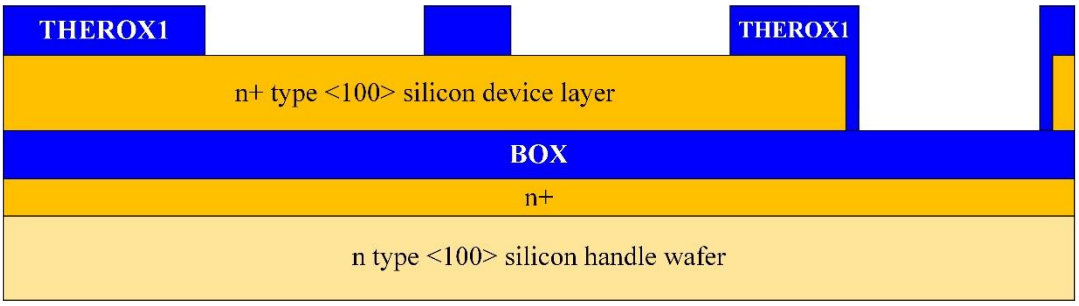


Figure 3.6. Patterning of THEROX1 layer with lithography and RIE (CHF3 + CF4) to define the active area.

Following the patterning of the THEROX1 layer, second thermal oxidation (THEROX2) is performed to construct the chemical and electrical isolation layer (Fig. 3.7). As mentioned above the thickness of the insulation layer is determined to be 100 nm. Therefore, this second oxidation step is planned to grow 100 nm oxide inside of the active area of the CMUT cells. In addition, it is planned to increase the thickness of the remaining thermal oxide at the outside of the active area by 30 nm.

This layer would provide the electrical isolation between the top electrode (conductive membrane, BNCD) and bottom electrode preventing any short circuit between the electrodes and enabling the operation of the device in collapse and collapse snap-back mode. Also, it provides full oxide coverage for device layer of the SOI wafer which is the bottom electrode of the CMUT device. This is essential since the polysilicon is removed in XeF_2 plasma during the sacrificial release and the device layer, which is made of silicon, would also etched away during this process step if it is not fully covered with a high quality oxide which acts as chemical isolation layer for this process step. Therefore, the second oxidation is realized with dry oxidation technique since the quality of the thermal oxide in the active area of the CMUT cell is paramount. In addition, the thickness of the THEROX2 layer is sufficiently low so it is feasible to grow the oxide with dry oxidation technique.

According to the thermal oxidation algorithm, it is required to grow oxide for 150 minutes at 1000 °C with dry oxidation to grow 100 nm thermal oxide on the silicon surface (in the active area of the CMUT cell). Also, this algorithm calculates that

with given receipt, in this second thermal oxidation process step, the thickness of the 220 nm thick thermal oxide at the outside of the active area would increase by 36.8 nm. Therefore, the final thickness of the THEROX1 layer would be approximately 250 nm which is the desired final thickness for this layer at the beginning.

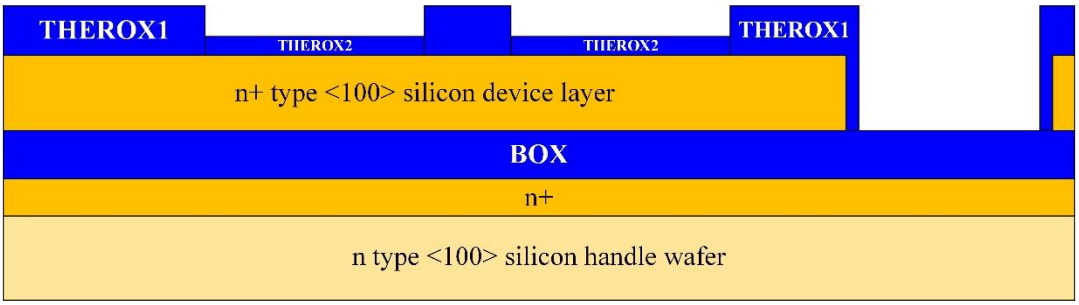


Figure 3.7. Thermal growth (100 nm) of the second thermal oxide (THEROX2) layer by dry oxidation to construct the electrical and chemical isolation layer. The thickness of the THEROX1 layer is increased to 250 nm.

After the second thermal oxide growth, the first sacrificial polysilicon layer (Poly1) is deposited by LPCVD. The Poly1 is the first sacrificial layer to fill the currently constructed cavity in the active area of the CMUT cells. Therefore, the deposition thickness of this layer is determined to be equal to the difference between the thicknesses of THEROX1 (250 nm) and THEROX2 (100 nm) layers which is 150 nm.

After the deposition, the polysilicon outside of the active area of the CMUT cells would be removed. The Poly1 layer is patterned with lithography and RIE (SF_6) (Fig. 3.8) where silicon dioxide is the etch stop. “ActiveArea-Mask#2” mask is used during the exposure of the photoresist, while lithography type is light.

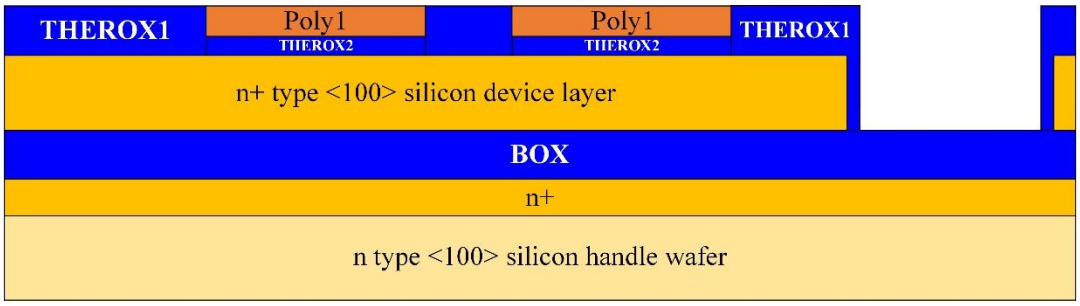


Figure 3.8. First polysilicon (Poly1) layer deposition (150 nm) by LPCVD and then patterning with lithography and RIE (SF_6) to remove polysilicon at the outside of the active area.

The etch hole for the sacrificial etching cannot be placed on the membrane since the CMUT will be operated in immersion. It should be placed near by the active area. Therefore, an etch channel, that is made of polysilicon, is required to create an etching path from etch hole to active area. For this purpose, after the Poly1 layer deposition and patterning, second sacrificial polysilicon layer (Poly2) is deposited by LPCVD. The deposition thickness is equal to etch channel height, which is 150 nm.

The Poly2 layer is the sacrificial layer to construct the required etch channels, and it will be chemically etched together with Poly1 during the sacrificial release of polysilicon. The polysilicon remaining in the active area will construct the CMUT gap. Considering the first sacrificial polysilicon layer, Poly1 that remains in the active area after the patterning the polysilicon thickness in the active area of the CMUT cell, after the deposition of the second polysilicon layer, Poly2, is equal to 300 nm which is the determined gap height value. Therefore, polysilicon remaining inside the active area, etch channel and the etch hole will be remaining until during the sacrificial release whereas the rest of the polysilicon should be removed after the deposition of the Poly2. Thus, deposition of second polysilicon layer is followed by patterning of polysilicon with lithography and RIE (SF_6) (Fig. 3.9). Silicon dioxide behaves as the etch stop for this RIE process. So that, as planned, the gap and the etch channel height will be 300 nm and 150 nm, respectively. “EtchChannel-

Mask#3" mask is used during the exposure of the photoresist, while lithography type is light.

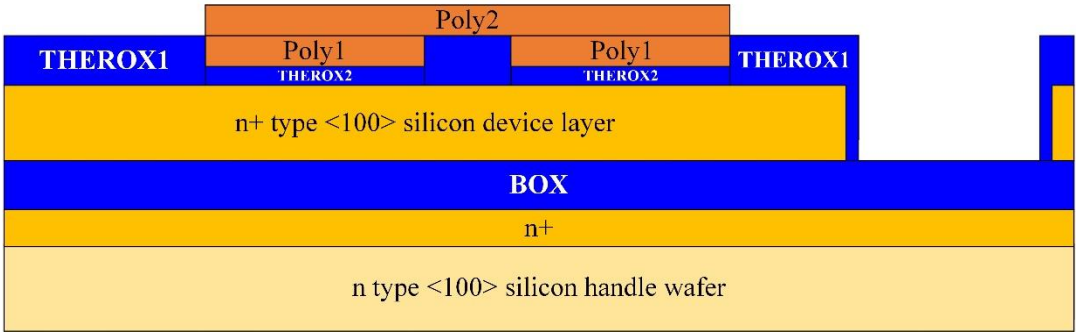


Figure 3.9. Second polysilicon (Poly2) deposition (150 nm) by LPCVD and then patterning with lithography and RIE (SF_6) to remove polysilicon at the outside of the active area, etch channel and etch hole.

Afterwards, the process continues with the deposition of highly boron doped NCD (BNCD) by HFCVD technique (Fig. 3.10). Since this is the membrane deposition, the deposition thickness is equal to membrane thickness which is determined to be 400 nm.

First, the seeding of carbon crystal on the wafer surface is realized in ultrasonic bath. Then the diamond is growth through those seeds by introducing a gaseous mixture with a certain receipt into the furnace where the receipt of the gaseous mixture effects the diamond film properties.

BNCD is the membrane material of the CMUT and thus there are some essential constraints about this deposition. First, it is beneficial to have conductive CMUT membrane since the metal connection to the diamond films might not be as successful as desired. During the high power operation of CMUT and the large membrane vibration, metal might break-off from the membrane due the low metal to the diamond stiction. Therefore, a metal top electrode where CMUT is featuring diamond membrane might not be reliable and a conductive membrane operating as the top electrode would be more preferable. Therefore, the conductivity of the BNCD

film (~0.02 Ω.cm) via boron doping is important. Another issue is the stress on the film. Since compressive stress causes buckling of the membrane and effect the operation of the device negatively whereas tensile stress alters the frequency bandwidth and operation of the device, low residual stress (<50 MPa) is essential. Hence, the thickness of the membrane effects the device operation and determined to be 400 nm for the developed microfabrication, it is important to realize as possible as uniform BNCD deposition. Otherwise, in a large array, the CMUT operation might alter from element to element which would affect the device operation adversely.

Another important note on diamond films is that diamond films might be burned above 600° C, in the existence of O_2. Therefore, for the safety and reliability of the microfabrication, from now on it beneficial to avoid any process step that is realized above 600° C.

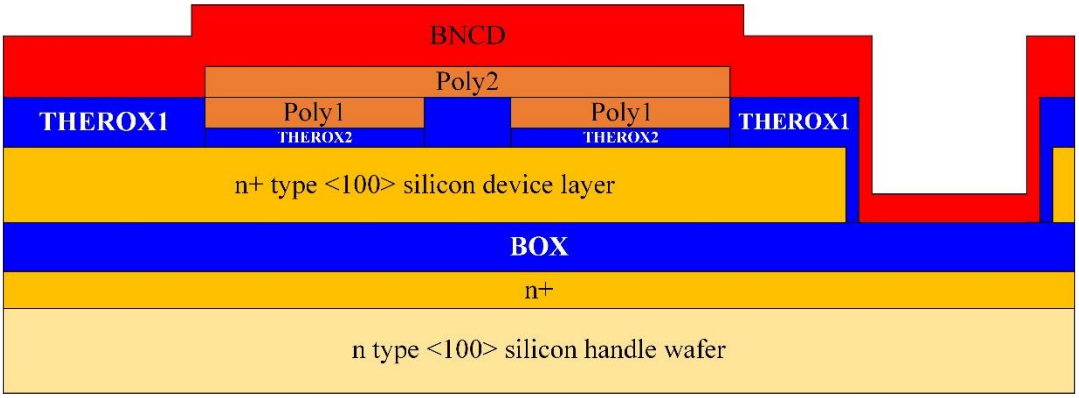


Figure 3.10. BNCD deposition (400 nm) by HFCVD.

Afterwards the BNCD deposition, BNCD is required to be patterned to define the etch hole, signal cavity and array isolation cavity. Etch hole enables XeF_2 plasma to enter into etch channel and CMUT cavity from the top surface of the wafer. Signal cavity is required to construct the via for providing the metal contact to the bottom electrode in the following process steps. Array isolation cavity is required to construct the isolation between CMUT array elements, providing grounded metal line between them and grounding the handle wafer where the area for array isolation

cavity is defined inside the trenches constructed during the RIE of the device layer. So diamond reaming inside these areas is required to be removed.

The plasma for RIE of the diamond films consists of O_2 and SF_6 where O_2 plasma etches photoresist and therefore, photoresist or any another organic film cannot be used as the masking material for any diamond RIE. Silicon dioxide is the common masking material for diamond RIE ($SF_6 + O_2$) in which the selectivity is good enough for a successful diamond patterning. Therefore, before the patterning of the BNCD, first the hard mask material LTO (LTOMASK) is deposited by LPCVD. The thickness of the LTOMASK layer is 400 nm, which is equal to thickness of the BNCD layer. After the deposition, the LTOMASK layer is patterned with lithography and RIE (CHF_3 + CF_4) (Fig. 3.11). "DiamondEtch-Mask#4" mask is used during the exposure of the photoresist, while lithography type is dark. The etch hole, signal cavity and the array isolation cavity are as depicted in Figure 3.11.

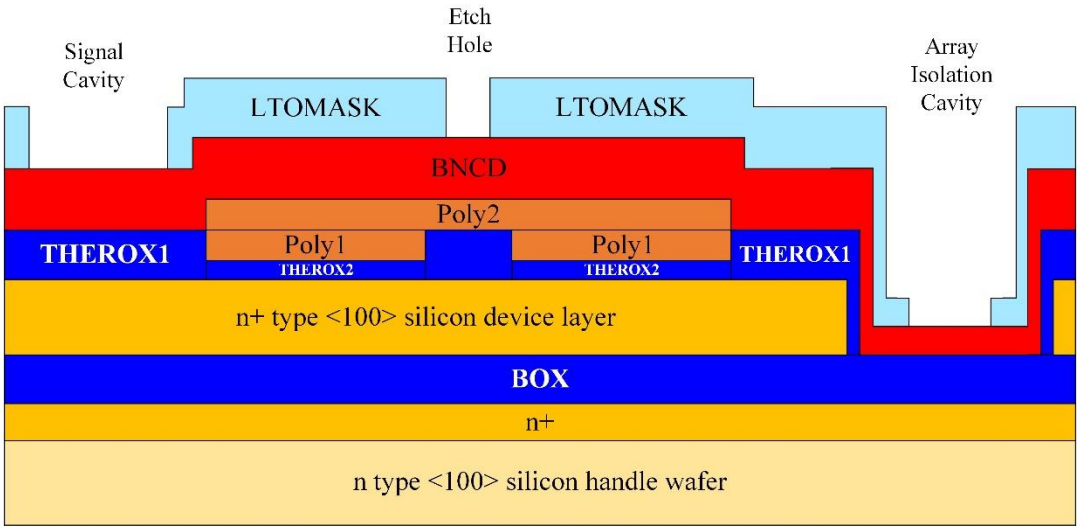


Figure 3.11. The LTO hard mask layer (LTOMASK) deposition (400 nm) by LPCVD followed by patterning of the layer with lithography and RIE (CHF_3 + CF_4).

Following the patterning of LTOMASK layer, BNCD is patterned with RIE (O_2) while LTO is being the hard mask material (Fig. 3.12). Silicon dioxide underneath the BNCD layer acts as an etch-stop for RIE of BNCD.

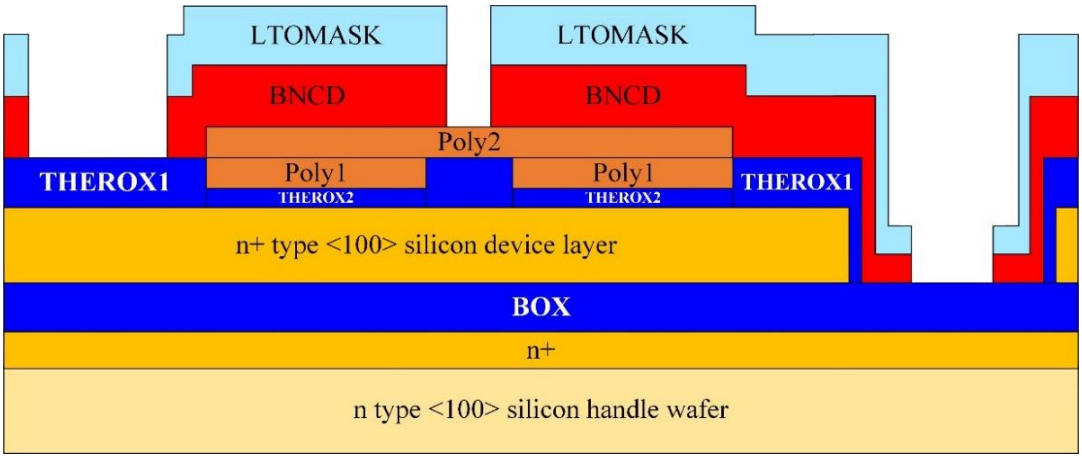


Figure 3.12. Patterning of BNCD with RIE (O_2) while LTO (LTOMASK) layer is being the hard mask.

Subsequently, the sacrificial etching of polysilicon in XeF_2 plasma is performed (Fig 3.13). In this step, sacrificial polysilicon layers Poly1 and Poly2 are removed whereas the device layer of the SOI wafer on which a high quality thermal silicon dioxide is growth that acts as a chemical isolation layer and the handle wafer that is covered with silicon dioxide from bottom, the silicon dioxide layers and BNCD are not etched (or etched by infinitesimal amounts). The selectivity of XeF_2 for polysilicon and thermal oxide was found out to be 1000:1 [94] whereas it does not etch BNCD at all, since diamond is a chemically inert material. The XeF_2 plasma enters into CMUT cavity through the etch hole and etch channel and etches polysilicon isotopically.

The required sacrificial etch time depends on the etch rate of polysilicon in XeF_2 and the maximum etch depth to release all the CMUT membranes. The maximum etch depth depends on the size of the largest membrane and the etch channel length. Furthermore, the size of the etch hole might affect the etch rate since XeF_2 plasma enter into structure through those holes. Therefore, the required etch time is changeable and some experiments on test wafers should done to determine the etching time and to optimize the etch time and consumption of XeF_2 according to the etch rate versus etch time data for a single pulse etching of XeF_2.

Dimples and CO_2 dry cleaning afterwards the sacrificial release is not performed since XeF_2 is a gaseous chemical in plasma form and this is a dry release process. Therefore, the risk for stiction of the membrane due to the capillary force is avoided.

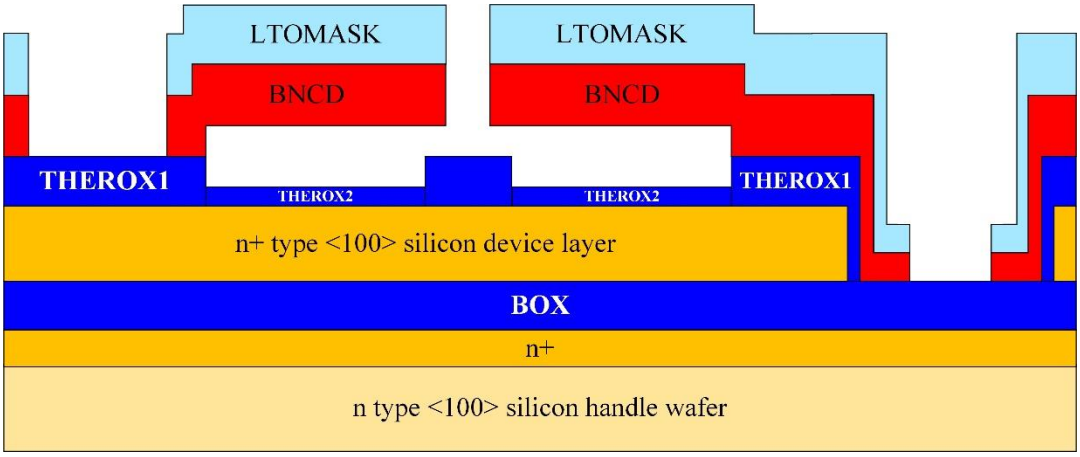


Figure 3.13. Sacrificial etching of polysilicon in XeF_2 plasma.

The CMUT cavities must be vacuum-sealed for successful operation of the device in immersion. Therefore, following the sacrificial release, sealing is performed by deposition of LTO (LTOSEAL) in LPCVD furnace (Fig. 3.14). The deposition amount is determined to be 150 nm which is the height of the etch channel so that sealing would occur in etch hole mouth of the etch channel with a high probability. It is beneficial to choose the sealing material with a high sticking coefficient such as LTO to seal the cavities with the least deposition into the CMUT cavities.

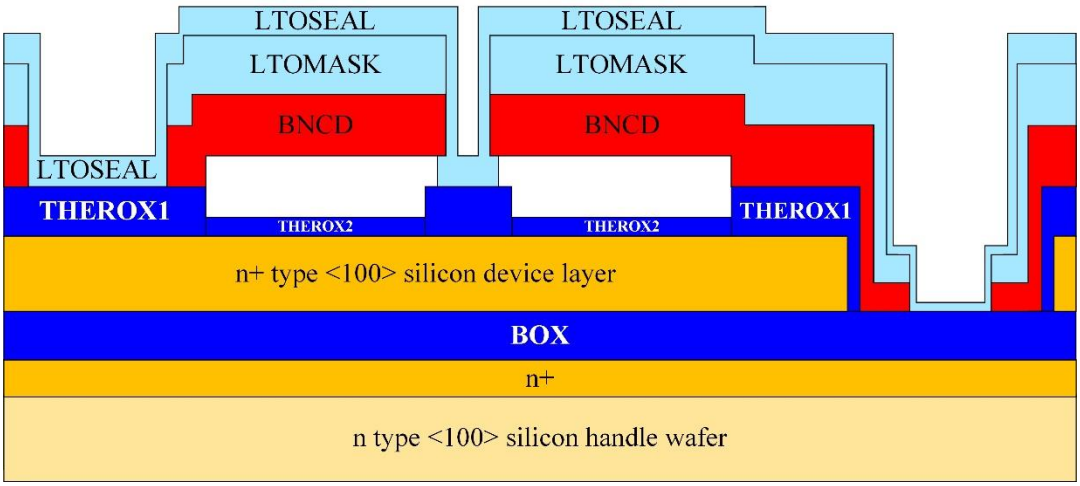


Figure 3.14. LTO (LTOSEAL) deposition (150 nm).

Subsequently, unnecessary silicon dioxide remaining in the structure should be removed. LTO remaining on the top of the membrane, oxide standing inside of the signal cavity and array isolation cavity are classified as unnecessary. For this purpose, lithography, and removal of oxide is performed (Fig. 3.15).

In additional to photoresist, BNCD is used as a masking material during the removal of silicon dioxide since any HF-based solutions cannot etch any diamond film (because diamond is a chemically inert material). So, while photoresist is covering silicon dioxide remaining in the etch hole, BNCD prevents etching of the silicon dioxide underneath it. The removal of silicon dioxide must be performed with BHF (Buffered HF) since photoresist is used as the masking material. BHF is applied to etch approximately 1.2 μm oxide. Furthermore, BHF etches silicon dioxide isotopically, which should be considered while designing the layout, since it will also etch 1.2 μm (at least) oxide underneath the BNCD and photoresist. Therefore, the coverage of BNCD and photoresist over the silicon dioxide on the layout masks should be designed accordingly. “EtchVia-Mask#5” mask is used during the exposure of the photoresist, while lithography type is light.

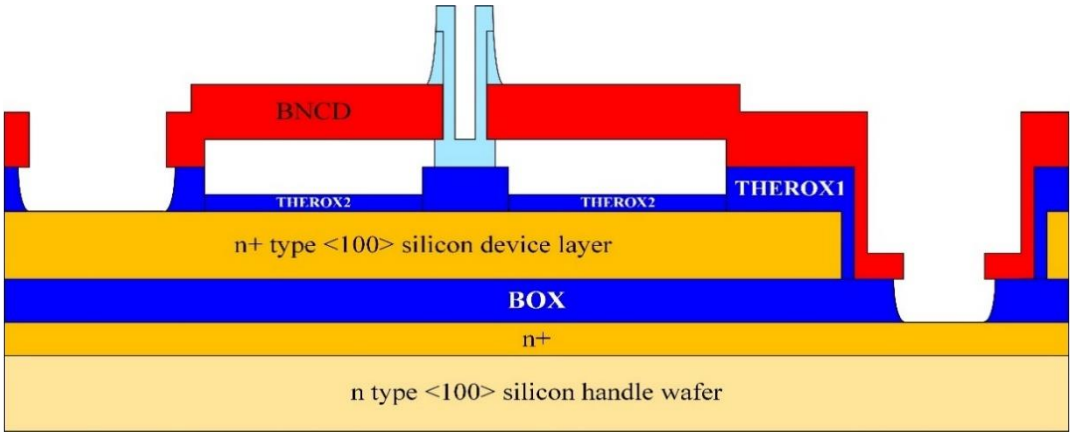


Figure 3.15. Removal of unnecessary silicon dioxide in BHF with lithography.

The next and the final step before dicing is the metallization (Fig. 3.16). Even though the CMUT membrane material BNCD is conductive and therefore a metal top electrode is not required, metal is required for providing the metal pad connections. Gold or Aluminum may not have solid contact with diamond films. Therefore, in this process step, tri-metal, 30 nm Titanium, 20 nm Copper, and 500 nm Gold are evaporated on the wafer, where Titanium and Copper provide stiction and diffusion layers, respectively. Gold is preferable as conductive layer since it is not oxidized, highly conductive and considering the gold wire-bonding it provides a good connection to pads on the printed circuit board (PCB). Patterning of the metal layer is performed by using the Metal lift-off technique. “Metal-Mask#6” mask is used during the exposure of photoresist while the lithography type is dark.

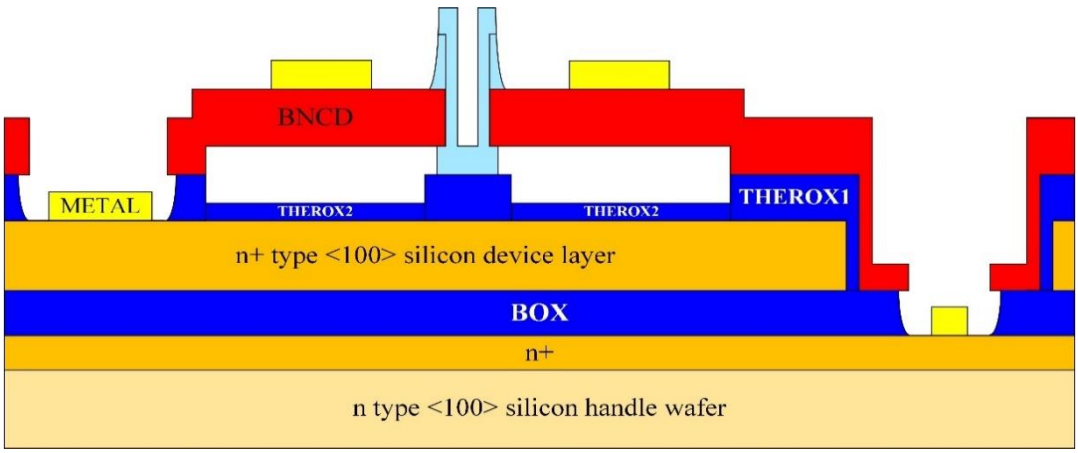


Figure 3.16. Tri-Metal deposition and patterning with Metal Lift-off technique.

3.2.2 The Summary of the Developed Microfabrication Process Flow

Table 3.2. Process flow of the developed microfabrication.

Step Number	Process Information
1	6-in n-type <100> SOI wafer (highly n-type doped 2 μm device layer, 1 μm buried oxide layer, at surface highly n-type doped 450 μm handle wafer)
2	Photoresist covering
3	Patterning of photoresist with, "BottomElectrode-Mask#1" (lithography type = LIGHT)
4	RIE (SF_6) for patterning the device layer of the SOI wafer
5	Removal of remaining photoresist and organics
6	Thermal oxidation (dry (30 min)/wet/dry (30 min)) (220 nm)
7	Photoresist covering
8	Patterning of photoresist with "ActiveArea-Mask#2" (lithography type = DARK)
9	RIE (CHF_3 + CF_4) for thermal oxide patterning
10	Removal of remaining photoresist
11	Thermal oxidation (dry) (100 nm)
12	Polysilicon deposition (150 nm) by LPCVD
13	Photoresist covering
14	Patterning of photoresist with "ActiveArea-Mask#2" (lithography type = LIGHT)
15	RIE (SF_6) for polysilicon patterning
16	Removal of remaining photoresist
17	Polysilicon deposition (150 nm) by LPCVD
18	Photoresist covering

Table 3.2. (Continued)

19	Patterning of photoresist with “EtchChannel-Mask#3”, (lithography type = LIGHT)
20	RIE (SF_6) for polysilicon patterning
21	Removal of remaining photoresist
22	BNCD deposition (400 nm) by HFCVD
23	LTO deposition (400 nm) by LPCVD
24	Photoresist covering
25	Patterning of photoresist with “DiamondEtch-Mask#4”, (lithography type = DARK)
26	RIE (CHF_3 + CF_4) for LTO patterning
27	Removal of remaining photoresist
28	RIE (SF_6 + O_2) for BNCD patterning
29	Sacrificial etch of polysilicon in XeF_2 plasma etchant
30	LTO deposition (150 nm) by LPCVD for sealing
31	Photoresist covering
32	Patterning of photoresist with “EtchVia-Mask#5”, (lithography type = LIGHT)
33	Removal of unnecessary silicon dioxide in BHF (1.2 μm)
34	Removal of remaining photoresist
35	Photoresist covering
36	Patterning of photoresist with “Metal-Mask#6”, (lithography type = DARK)
37	30 nm Ti + 20 nm Cu + 500 nm Au deposition by evaporation
38	Patterning of metal layer by removal of the photoresist (Metal Lift-off)
39	Dicing

Table 3.3. Material, thickness (nm), deposition type and layer type of layers.

Layer Name	Material Type	Thickness (nm)	Deposition Type	Layer Type
Device Layer	Highly n type doped crystal silicon	2,000	-	Structural
THEROX1	Silicon dioxide	250	Thermal Growth	Structural
THEROX2	Silicon dioxide	100	Thermal Growth	Structural
Poly1	Polysilicon	150	LPCVD	Sacrificial
Poly2	Polysilicon	150	LPCVD	Sacrificial
BNCD	Highly Boron doped Diamond	400	HFCVD	Structural
LTOMASK	LTO	400	LPCVD	Hard Mask
LTO_S	LTO	150	LPCVD	Sealing
METAL	Ti + Cu + Au	500	Evaporation	Structural

Table 3.4. Affected layer(s), masking material, lithography mask and field type of each RIE or patterning processes.

Process	Layer(s) affected	Masking Material	Lithography Mask	Field Type
Silicon crystal RIE	Device Layer	Photoresist	"BottomElectrode-Mask#1"	LIGHT
Silicon dioxide RIE ($CHF_3 + CF_4$)	THEROX1	Photoresist	"ActiveArea-Mask#2"	DARK
Polysilicon RIE (SF_6)	Poly1	Photoresist	"ActiveArea-Mask#2"	LIGHT
Polysilicon RIE (SF_6)	Poly2	Photoresist	"EtchChannel-Mask#3"	LIGHT
LTO RIE ($CHF_3 + CF_4$)	LTOMASK	Photoresist	"DiamondEtch-Mask#4"	DARK
BNCD RIE ($SF_6 + O_2$)	BNCD	LTO	-	-
Metal Lift-off	METAL	Photoresist	"Metal-Mask#6"	DARK

Table 3.5. Etch type, affected and unaffected layers of each chemical etching processes.

Process	Etch Type	Layer(s) affected	Unaffected Layers
Sacrificial etching with XeF_2 plasma etchant	Dry-plasma	Poly1 (Removed) Poly2 (Removed)	Device Layer THEROX1 THEROX2 BNCD LTOMASK
Wet etching of unnecessary silicon dioxide in BHF	Wet	LTOSEAL LTOMASK THEROX1	Device Layer THEROX2 BNCD

Table 3.6. Field type and purpose of lithography masks.

Mask Name	Field Type	Purpose
"BottomElectrode-Mask#1"	LIGHT	Patterning of device layer of the SOI wafer
"ActiveArea-Mask#2"	DARK	Patterning of THEROX1 layer
	LIGHT	Patterning of Poly1 layer
"EtchChannel-Mask#3"	LIGHT	Patterning of Poly2 layer
"DiamondEtch-Mask#4"	DARK	Patterning of LTOMASK layer and BNCD layer
"EtchVia-Mask#5	LIGHT	Etching of unnecessary silicon dioxide
"Metal-Mask#6"	DARK	Patterning of ~500 nm Tri-Metal layer

3.3 CMUT Array Design and Mask Layout

Design of the 1-D CMUT arrays were done with a script developed on MATLAB. The developed MATLAB script requires the parameters about the design to be determined and entered by the user. In accordance, it calculates the position and size of each feature and repeating (repeating amount and distance in x and y direction) of some previously drawn features in the layout. Afterwards, it outputs a text document consists of a list of commands that realize the drawing of those features in the Semulator3D Layout Editor 9.0 (.cat file) released by Coventor (North Carolina, USA) automatically. Furthermore, the layout design is automatically exported to Tanner L-EDIT software (.gds file) released by Mentor Graphics Corporation (Wilsonville, USA).

Two identical 64-element 1D CMUT arrays, both capable of working as HIFU and FAST array, were designed on top of each other on the same dice. As mentioned above, these two identical arrays were designed to operate as a, HIFU array operating around 2 MHz in collapse-snapback mode and as an FAST array operating 8 MHz in collapse mode. It is reasonable to operate HIFU array in collapse-snapback mode since the main aim of an HIFU array is generating high power where the collapse-snapback mode is classified high power transmission operation of a CMUT [42-43]. Also, the aim of the FAST array is generating and sensing Ultrasound waves at high frequency and high efficiency where the collapse mode of CMUT is providing high frequency and high efficiency as mentioned in literature [44]. The layout design and of two neighboring 64-element CMUT arrays is as depicted in Figure 3.17.

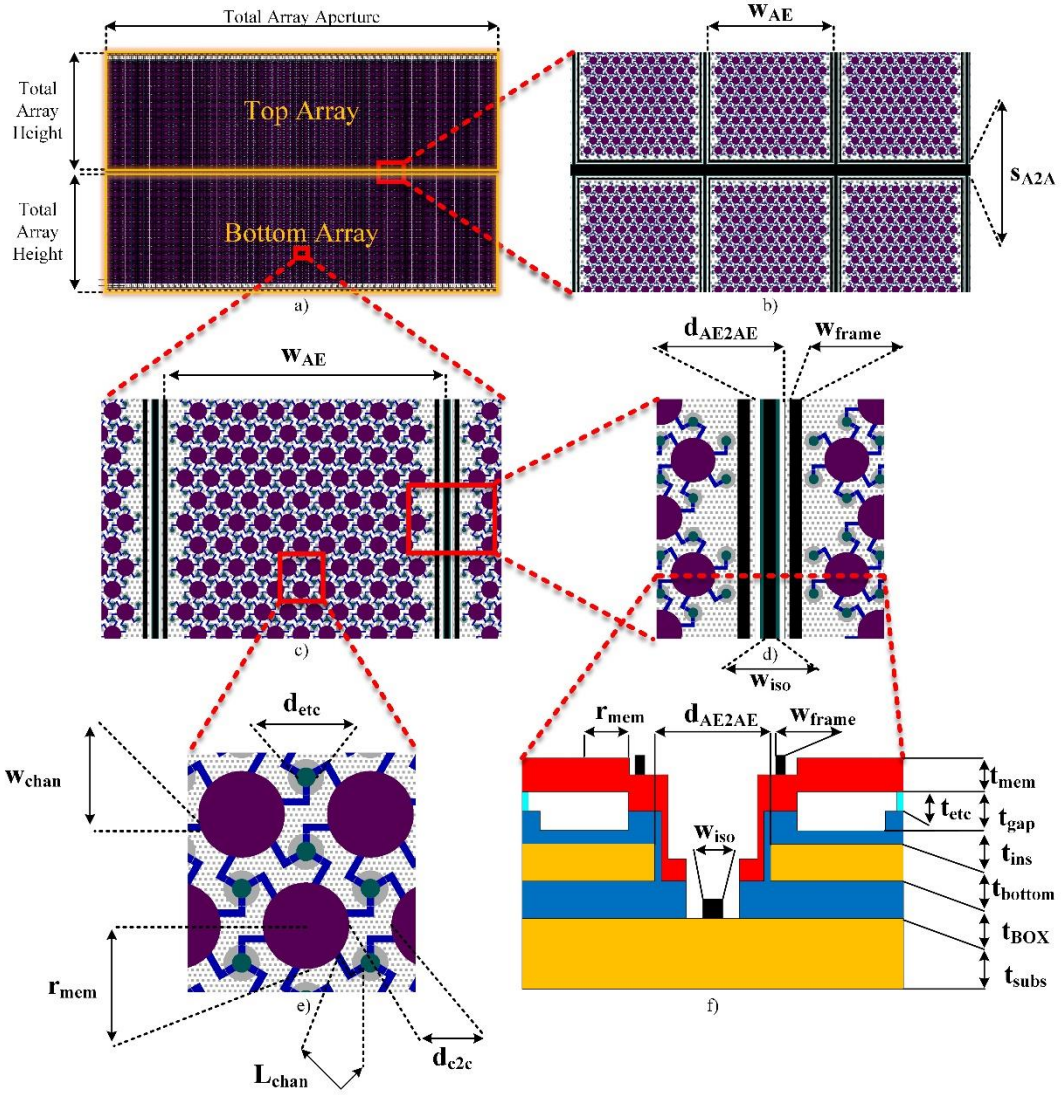


Figure 3.17. (a) The overall layout design of two identical neighboring 64-element CMUT array. (b) Magnified view at isolation between two neighboring CMUT arrays. (c) Magnified view at a single array element. (d) Magnified view at isolation between two neighboring array elements. (e) Magnified view at 3 neighboring CMUT cells in an array element. (f) Representative 2D cross sectional view of CMUT.

As explained above in detail there 6 masks in total. The “BottomElectrode-Mask#1” mask is shown with black dots on white back ground, the “ActvieArea-Mask#2” mask is shown with purple, the “EtchChannel-Mask#3” mask is shown with blue,

the “DiamondEtch-Mask#4” mask is shown with green, the “EtchVia-Mask#5” mask is shown with gray and the “Metal-Mask#6” mask is shown with black features.

The orientation of CMUT cells was determined to be as depicted in Figure 3.42.f. where each neighboring 3 CMUT cells were oriented to construct an equilateral triangle. Therefore, according to the this mentioned orientation, if the maximum number of CMUT cells in a single row of an array element is N, then the minimum number of CMUT cells in a single row of an array element is N-1 and from top to bottom the number of CMUT cells per row follows as N, N - 1, N, N – 1, N. There are 6 etch channels and etch holes framing a single CMUT cell that are in common use with other neighboring CMUT cells. The parameters and their values of CMUT cell and array is as given in Table 3.7.

The frame metal is the metal line that is specific to an array element frames the array element and carries the ground signal throughout the array element. The width of this line effects the resistance of the array and thus, it should be at large enough. Therefore, in the design the frame metal width (w_{frame}) was determined as 10 μm. Similar logic is valid for the isolation lines (placed between neighboring array elements) that carries ground signal, and therefore, the width of isolation lines (w_{iso}) was chosen as 10 μm.

The size of the signal pad and grounding pad and the distance between them was determined according to the future processes, wire bonding and PCB design. According to the wire bonding design guide of Würth Elektronik (Baden-Württemberg, Germany), the pad size should be at least 80 μm, whereas the pad repeating should be at least 250 μm. Therefore, in the design, the widths of pads were determined as 100 μm whereas the repeating of pads were determined to be at least 300 μm in total.

Table 3.7. The cell and array parameters and their values.

Parameter	Value
Number of Array Elements	64
Total Array Aperture, cm	3.92
Total Array Height, mm	8.95
Cells per element	808
Maximum cells per single row of element	10
Top array to bottom array separation (s_{A2A}), μm	64
Array Element width (w_{AE}), μm	583.94
Array Element to Array Element distance (d_{AE2AE}), μm	24
Isolation metal width (w_{iso}), μm	10
Frame metal width (w_{frame}), μm	10
Cell radius (r_{mem}), μm	18
Cell to cell distance (d_{c2c}), μm	17.69
Substrate thickness (t_{subs}), μm	450
BOX layer thickness (t_{BOX}), μm	1
Bottom electrode thickness (t_{bottom}), μm	2
Insulator layer thickness (t_{ins}), nm	100
Gap thickness (t_{gap}), nm	300
Etch channel thickness (t_{etc}), nm	150
Membrane thickness (t_{mem}), nm	400
Etch hole diameter (d_{etc}), μm	8
Etch channel width (w_{chan}), μm	3
Etch channel average length (L_{chan}), μm	15
Signal pad size, (height) μm x (width) μm	120 x 100
Ground pad size, (height) μm x (width) μm	100 x 100
Signal pad to Ground pad distance, μm	203.97

Bottom electrodes of array element are isolated from each other since the array is designed to operate in immersion and therefore the signal will be given to bottom electrode. Due to this reason, each element has individual two (signal and ground) pads. Therefore, the array element repeating should be higher than 600 μm (2 times the repeating of metal pads). In addition to this information, without disturbing the orientation of the CMUT cells in an element, the maximum number of cells in a single row of an element and the array element width (w_{AE}) are determined to be 10, and 583.94 μm, respectively. Considering the array element repeating (which is 607.94 μm), the final pad repeating value is 303.97 μm.

Considering the previous etch hole studies [39-40], the minimum etch hole radius should be 2 μm for providing a successful sacrificial release and sealing. For a safe process (sacrificial release and sealing) considering the minimum grid number for commercial process that they provide (which is 2 μm) the radius of etch hole ($d_{etc}/2$) was determined to be 4 μm. In accordance with this information and decision, the etch channel width was chosen as 3 μm where the average channel length (the length of the channel calculated from the mid-line of the channel) is 15 μm. Therefore, considering the orientation of cells and etch holes, and the size of cells, etch holes and channels, the minimum distance between cell to cell was calculated and determined as 17.69 μm.

The "BottomElectrode-Mask#1" mask, given in Figure 3.18(a), is for constructing the bottom electrodes of each array element and is has a lithography type of LIGHT. Therefore, the inside of these features would represent the bottom electrodes. The silicon outside of these features would be etched away and trenches between bottom electrodes would be constructed on 2 μm device layer. Furthermore, in this mask, to prevent the loading and provide uniform etching as much as possible, the silicon outside of the locations where arrays were located, with some distance between silicon and arrays, should also be covered with photoresist throughout the wafer during silicon patterning. For this reason, in the full wafer layout, additional features outside of the arrays, with some distance to arrays, were also drawn in this mask layout. However, the top and bottom arrays are close enough to not consider the

loading effect that is mentioned, so that wide trenches between them can be constructed. In Figure 3.18(a), the wide trench represents isolation between top and bottom neighboring arrays whereas the narrow trenches represent the isolation between array elements.

The “ActvieArea-Mask#2” mask, given in Figure 3.18(b), is for constructing the cavity of CMUT cells by etching oxide inside the active areas and filling the first polysilicon layer inside these areas. Therefore, during the oxide patterning it has a lithography type of DARK whereas in Poly1 patterning it has lithography type of LIGHT. Therefore, the inside of each feature drawn in this mask should represent the active area of each CMUT cell. The loading effect is not a concern for this mask, since this mask is used as DARK and LIGHT for different process steps and the etch amounts are considerably low. Therefore, in the full wafer layout, there was no need for additional features at the outside of the arrays.

The “EtchChannel-Mask3” mask, given in Figure 3.18(c), is for constructing the etch channels. As mentioned in above parts, this mask is used for patterning of the second sacrificial polysilicon layer, where polysilicon should be etched away at the outside of the active areas, etch channels and etch holes in which the mask lithography type is LIGHT. Therefore, same circular features that define the active areas in “ActiveArea-Mask#2” mask were drawn in this mask as well. In the full wafer layout, additional features outside of the arrays, with some distance to arrays, were also drawn in this mask layout, since the mask type is LIGHT to prevent the mentioned loading effect and provide uniform etching as much as possible.

The “DiamondEtch-Mask#4” mask, given in Figure 3.18(d), is for diamond patterning. The type of this mask is DARK and therefore, the inside of the features drawn on this mask represent the areas where diamond would be etched away. So, in this mask, features that represent etch holes, signal cavity areas and array isolation areas were drawn. The etch holes were defined in “EtchChannel-Mask3”, with circular shapes as shown in Figure 3.20(c). To construct the etch holes with same circular shapes at the same positions were drawn in this mask as well. Furthermore,

the isotropic etching of oxide in BHF process step, approximately 1.2 μm oxide underneath the diamond would also be etched. Considering the mentioned fact, the possible glide of photoresist at the edge of trench due to viscosity and manufacturing grid size, the distance between bottom electrode features in "BottomElectrode-Mask#1" mask and the array isolation features drawn in "DiamondEtch-Mask#4" was determined to be 4 μm.

The "EtchVia-Mask#5" mask, given in Figure 3.18(e), is for preventing the etching of structural oxide during the removal of unnecessary oxide in BHF process step. As mentioned above, in this process step, the structural oxide underneath the diamond layer would be protected. However, photoresist is required as well, since diamond was etched inside the etch holes, and CMUT cavities were sealed from etch hole entrance of the etch channels. Therefore, in this mask the oxide in etch holes should be covered with photoresist. In the mask, features that cover the etch holes were drawn since the lithography type is LIGHT. Considering the fact that oxide underneath the photoresist would be etched (~1.2 μm) due to isotropic etching, and the manufacturing grid size, it was determined that the circular shapes drawn in this mask should have the same center position as the circular etch hole features drawn in the previous masks while having 3.5 μm higher radius than those circular features.

The "Metal-Mask#6" mask, given in Figure 3.18(f), is for patterning of the metal. The features in this mask represent the metal pads and lines since the patterning is realized with Metal Lift-off technique and the lithography type is DARK. There is one signal (connected to the bottom electrode) and one ground (connected to the top electrode/membrane) pad for each array element in which the ground pad is connected to the frame metal which frames the whole array element and carries the grounding signal to decrease the resistivity of the array element. The distance between the frame metal and the edge of trench (bottom electrode) was determined to be 4 μm considering the possible glide of photoresist at the edge of trench due to viscosity and manufacturing grid size. Furthermore, taking the processing inside trench and manufacturing grid size into calculations, the cover of diamond etching

features on metal features (for signal pad and isolation line) was determined to be 3 µm.

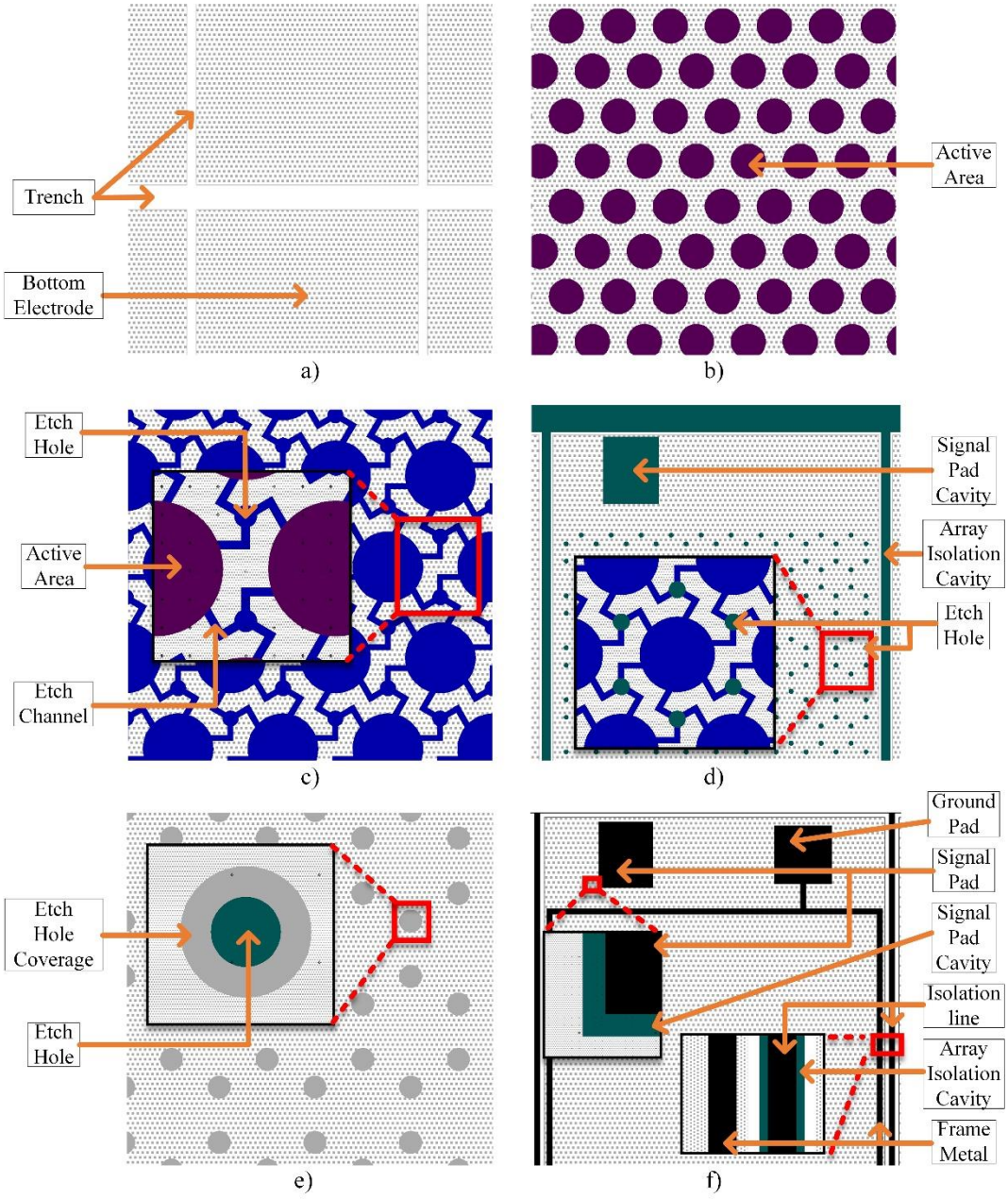


Figure 3.18. (a) "BottomElectrode-Mask#1", (b) "ActiveArea-Mask#2", (c) "EtchChannel-Mask#3", (d) "DiamondEtch-Mask#4", (e) "EtchVia-Mask#5" , and (f) "Metal-Mask#6" mask layouts.

The possible registration problem during the alignment of the masks does not affect the reliability of the microfabrication. During the design of the layout masks, the possible mismatch of 2 μm between any masks were considered as seen in Figure 3.18. Also, the mismatch in the alignment of the layout masks that uses the same active area features for patterning of first thermal oxide, patterning of first and second sacrificial polysilicon layer and same etch hole features for patterning of first polysilicon layer and diamond patterning would not affect the reliability of the microfabrication since the features sizes are higher than 2 μm and therefore considering that this is a sacrificial release process, any alignment mismatches are tolerable.

3.4 Virtual Microfabrication

3.4.1 Process Development and Virtualization on Semulator3D

Beforehand the microfabrication of the CMUT arrays, for verifying the developed microfabrication and the mask design, the visualization of the structure in the computer environment was essential. For this reason, commercially available Semulator3D 9.0 (Coventor, North Carolina) was used, which is a powerful semiconductor and MEMS processing simulator. This program offers advanced processing techniques such as bonding, thermal oxidation, RIE, deposition, lift-off, that was helpful to realize realistic microfabrication of CMUT arrays in the computer environment. In addition, it is possible to examine any possible failure due to any misinterpretation throughout the microfabrication using the built 3-D view of the structure that is provided after each process step by the simulation program.

First, the diamond material was defined in the material list since it is not defined in the material database of Semulator3D. In the Semulator3D, materials can be defined as either conductor or dielectric. Even though diamond is a semiconductor material, BNCD was defined as a conductor material with a resistivity value of 0.02 Ω.cm, which was the desired resistivity value for the diamond film deposition.

Afterwards, the process flow of the developed microfabrication was defined using the process steps defined in the process library database of Semulator3D. The process flow started with construction of the SOI wafer (the thickness of the handle wafer was defined as 3 μm for ease of the simulation and computational power). Then it continued according to the process flow given in Table 3.2.

In the simulation program, in addition to the process flow, the description of each process step is required to be defined. In Semulator3D, descriptiona of all growth, deposition and etching process steps are based on the amount. Therefore, the rate and time of the deposition, etch and growth are not used during the modeling. For some widely used process steps such as thermal oxide growth, metal lift-off, Semulator3D provides a receipt.

The pre-defined receipt of thermal oxidation modeling in Semulator3D uses interface growth between silicon and medium with growth fraction of 0.44 into silicon. The first thermal oxidation step (Step-6), was defined accordingly with growth amount of 0.22 μm. However, the second thermal oxidation (Step-11) was modeled a bit different from the receipt since a considerable amount of thermal oxide would be growth at silicon and thermal oxide interface. The modeling of the second thermal oxidation was performed in three steps. In the first step, growth of thermal oxide at silicon to thermal oxide interface was modeled with a growth amount of 0.03 μm and growth fraction of 0.44 into silicon. In the second step, growth of thermal oxide at thermal oxide to medium interface was modeled with a growth amount of 0.03 μm and growth fraction of 0.44 into thermal oxide. In the third and final step, the growth of thermal oxide at the silicon and medium interface was modeled with a growth amount of 0.1 μm and growth fraction of 0.44 into silicon.

The pre-defined receipt of metal lift-off in Semulator3D follows the sequence of deposition, exposure and development of photoresist, evaporation of metal and stripping of the photoresist and metal. In the receipt, the deposition of the photoresist was modeled as smooth planarizing deposition with deposition thickness of 1 μm and smoothing radius of 0.1. The exposure of the photoresist was modeled as

converting the photoresist material into exposed photoresist (defined as “ResistExp” in the material list), in the specified areas on the wafer according to mask and mask polarity. The development of the photoresist was modeled as the removal of the “ResistExp” material. The evaporation of the tri-metal was modeled as straight deposition of 500 nm gold (titanium and copper were not modeled due to low thickness). Finally, the pre-defined “Lift-off” process step found in the process library in Semulator3D was used for patterning the metal. This step strips out the material and the material overhead. The resist was chosen as the removal material.

For other process steps, found in the process flow of the “ULTRAMEMS Sacrificial Release Microfabrication”, lithography, LPCVD deposition and RIE of polysilicon and silicon dioxide and oxide removal in BHF, the descriptions were done base on the similar process steps found in some other pre-defined processes in the Semulator3D.

The lithography was defined in the same way it was defined for the metal lift-off process step that was explained above in detail. The LPCVD polysilicon and LTO depositions were defined using the conformal deposition tool in Semulator3D as they were modeled in the pre-defined process in Semulator3D. The lateral ratios of polysilicon and LTO depositions were determined as 1.0 and 0.8, respectively. The RIE patterning of polysilicon and LTO depositions were defined using the legacy basic etch tool in Semulator3D as they were modeled in the pre-defined process. In the developed microfabrication modeling, the lateral ratios of polysilicon and LTO etching were determined as 0.05 and 0.1, respectively. The etching amount were determined as 10 to 20 % more than the thickness of the film that is being patterning. The selectivity of polysilicon and LTO RIE over the other materials were disabled for the ease of the simulation and selectivity in RIE are miniscule in general. The oxide removal in BHF was modeled using the enhanced basic etching tool in Semulator3D where the etching amount and lateral ratio were entered as 1.2 μm and 1.0 (isotropic etching), respectively. The selectivity was enabled and the selectivity values over other materials were entered according to pre-defined BHF etching found in other pre-defined processes in Semulator3D.

For remaining process steps in the process flow of the "ULTRAMEMS Sacrificial Release Microfabrication", diamond deposition and RIE, and sacrificial etching of polysilicon in XeF_2 plasma, the steps were modeled according to the descriptions found in literature.

As mentioned above in detail, diamond deposition consists of two steps which are seeding and growth. However, since there is no process tool in Semulator3D to model seeding and growth of a material through seeding, the diamond deposition was modeled using the conformal deposition tool since isotropic growth was assumed [63,65,66]. Considering the fact that seeding at lateral surface is less probable the lateral ratio of the deposition was chosen as 0.2 to model the growth at the lateral surfaces. The RIE of diamond was modeled using the legacy basic etch tool in Semulator3D. The RIE amount was determined to be 10 % more than the diamond film thickness. Since diamond patterning is an essential process step, here the selectivity was enabled and the selectivity over other materials were defined according to the literature survey [46,70]. The selectivity over the hard mask material LTO was entered as 1:6.

The XeF_2 etching was modeled using the enhanced basic etch tool in Semulator3D. The lateral ratio of the etching was entered as 1.0 since this is isotropic chemical etch. Considering the total etch channel length and radius of CMUT cell, to remove all the polysilicon inside the active area, the etching amount was selected as 40 μm. The selectivity of the etching was enabled and selectivity over other materials were entered according to the literature survey [69,71,72]. Correspondingly, the selectivity over LTO and thermal oxide were defined as 0.005 (1:200) and 0.001 (1:1000).

The sealing deposition modeling was different than the standard LTO deposition modeling, since sealing would occur at the etch hole mouth of the etch channels. For this purpose, sealing was defined as sequence of steps. In the first step a mask operation was performed to define the etch holes by taking the intersection of "DiamondEtch-Mask#4" and "EtchVia-Mask#5". After that conformal deposition

having lateral ratio of 0.8 inside the etch holes with a deposition thickness of 0.05 μm were performed 3 times. Therefore, sealing at the etch hole mouth of etch channels were modeled step-by-step. The final step to truly model the sealing deposition was the conformal deposition of LTO having a lateral ratio of 0.8 at the outside of the etch holes with a deposition thickness of 0.15 μm.

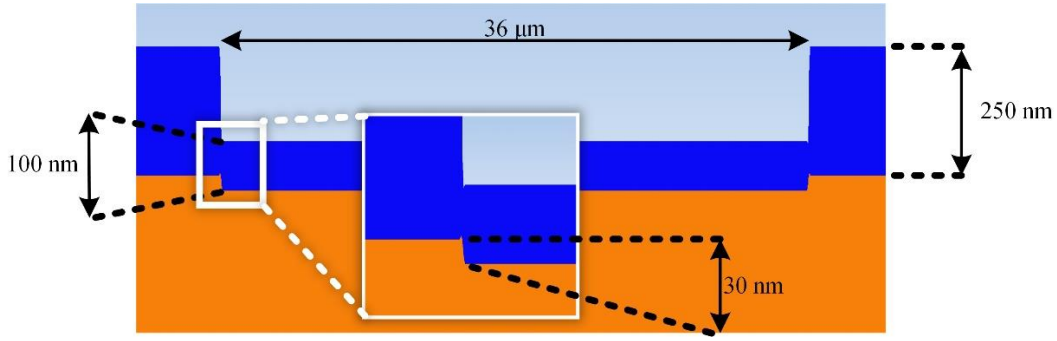


Figure 3.19. The virtualized structure after second thermal oxidation step (Step-11).

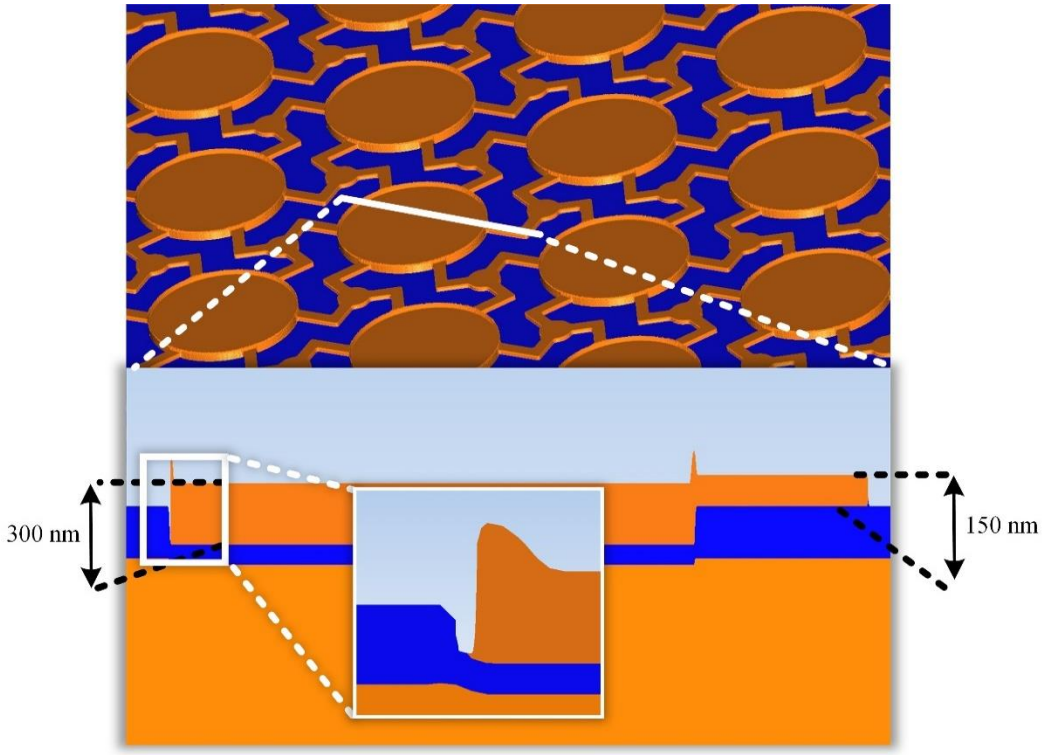


Figure 3.20. The virtualized structure after patterning of second polysilicon layer (Step-21).

As it can be seen from Figure 3.19, the cavities with a 100 nm oxide insulation layer were modeled without any defect. It is observed that oxide delves deeper into substrate by 30 nm in the active area compared to outside of this area.

As it was aimed, continuous sacrificial polysilicon layer that has a thickness of 300 nm in CMUT cavities and 150 nm in etch channels are observed in Figure 3.20. As it is expected, a polysilicon bump is occurred at the edges of the active area due to lateral deposition. Moreover, the closer view at the edge of active area is investigated. Even though, there is small mismatch between the oxide edge and polysilicon edge of active area is observed due to lateral etching in RIE and selectivity over other materials, this would not affect the solidity of microfabrication.

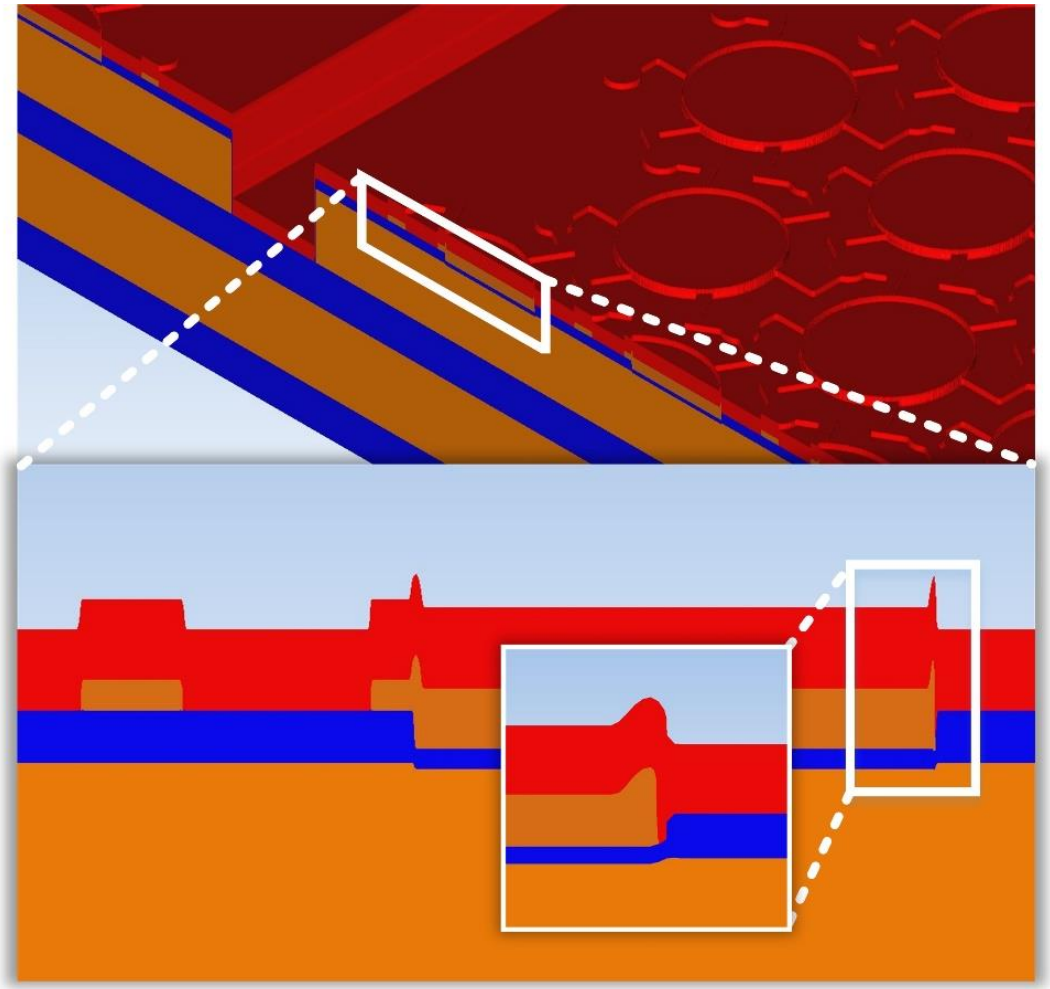


Figure 3.21. The virtualized structure after diamond deposition (Step-22).

As it seen in Figure 3.21, the diamond deposition with less deposition in the lateral surfaces of trenches is observed. The bump in the underlying polysilicon layer is transferred to diamond layer as expected. Furthermore, the narrow aperture due to mismatch between oxide edge and polysilicon edge of active area is completely filled by diamond since the width of the aperture is much smaller than the diamond deposition.

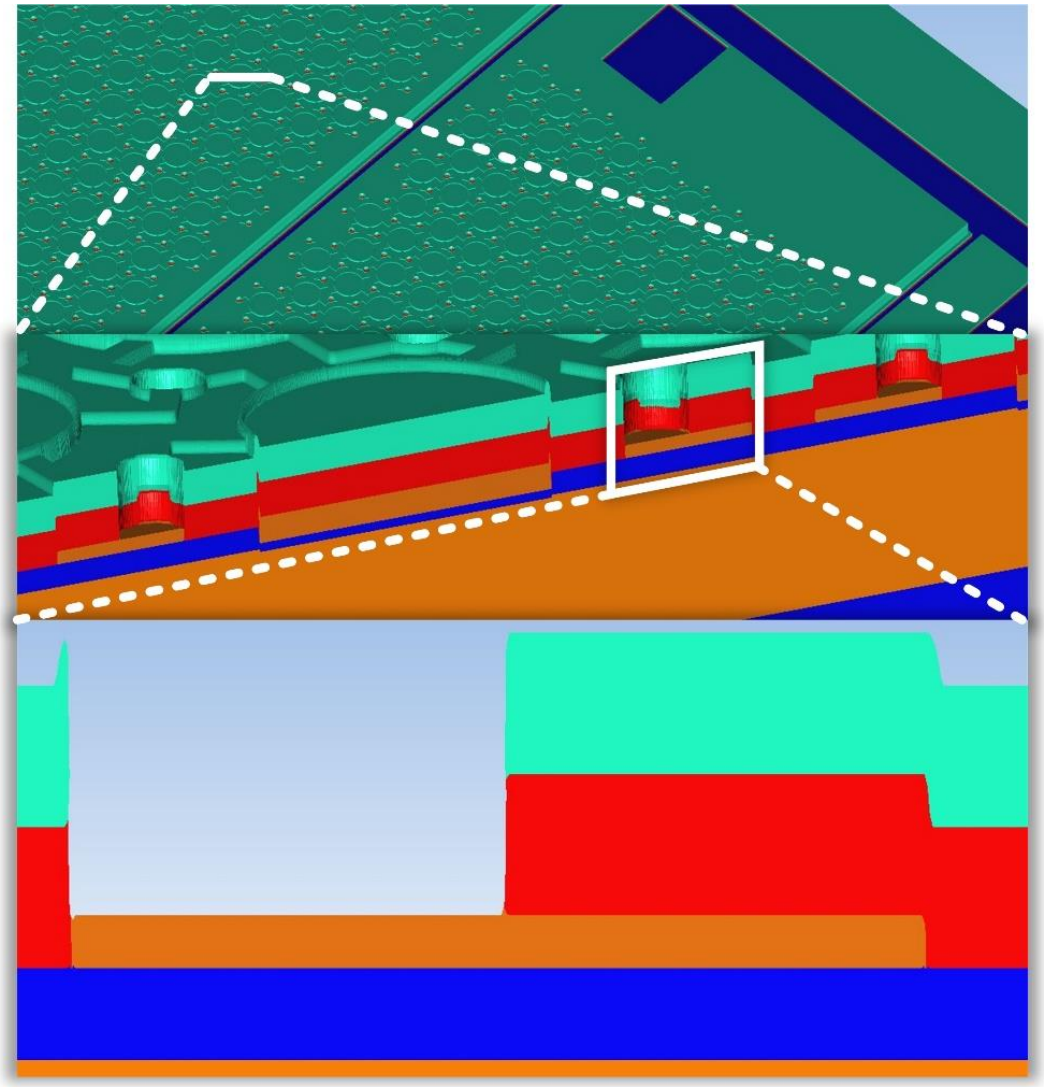


Figure 3.22. The virtualized structure after patterning of diamond while LTO being hard mask (Step-28).

The etch vias are constructed with diamond patterning as seen in Figure 3.22. As it was aimed for diamond is etched away down through the underlying polysilicon layer in etch vias. Even though the etch rate of the diamond might differ by the feature size, and it might be slower to etch diamond in etch via compared to signal cavity (as the feature for the signal cavity is higher than etch via), since there is thermal oxide under the diamond in array isolation and signal cavity areas this would not affect the solidity of the microfabrication.

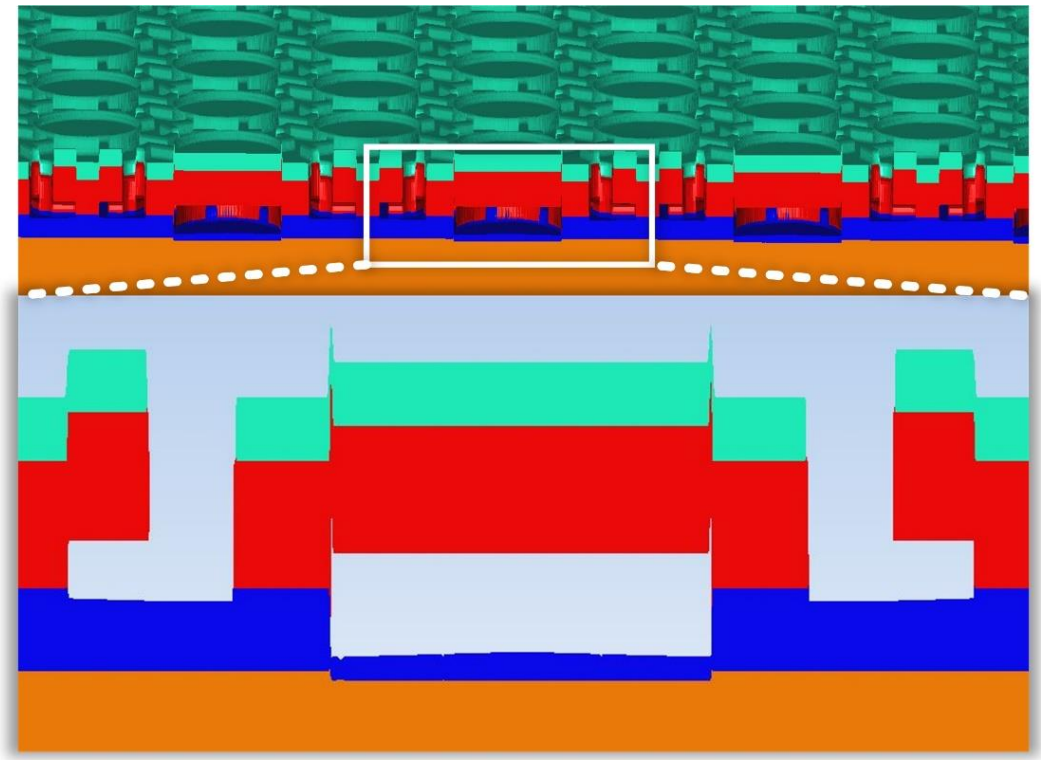


Figure 3.23. The virtualized structure after sacrificial polysilicon etching in XeF_2 plasma (Step-29).

The sacrificial release of diamond membrane by sacrificial etching of polysilicon in XeF_2 plasma is constructed as seen in Figure 3.23. There is a negligible amount thermal oxide etching during this process. The highest and lowest thickness of oxide are observed as 86 nm and 70 nm, respectively.

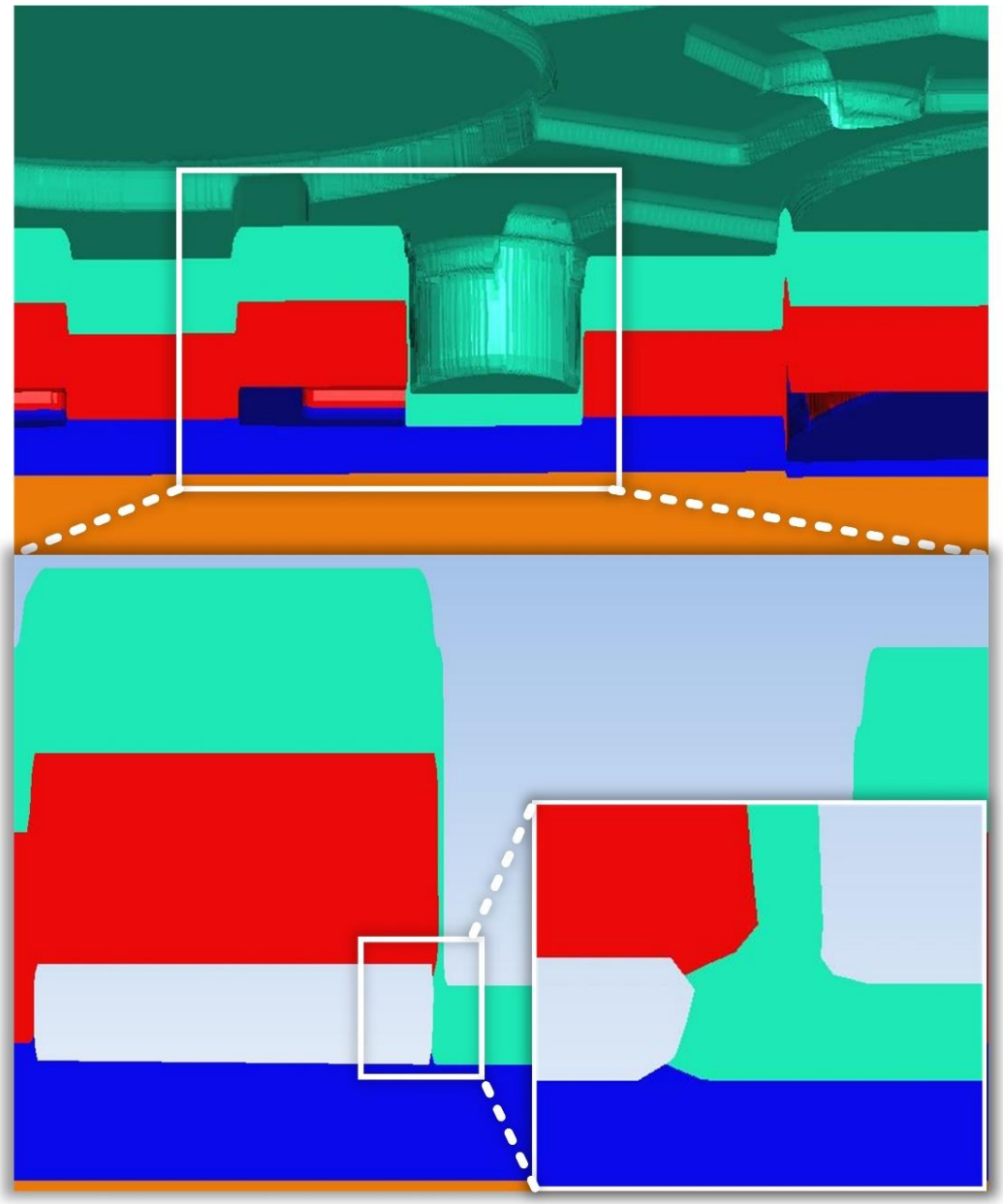


Figure 3.24. The virtualized structure after LTO deposition for sealing (Step-30).

As seen from Figure 3.24, the sealing of CMUT cavities from the etch hole month of the etch channels was constructed. It was assumed that LTO deposition inside the active area and etch channel would be insignificant, since LTO has a low sticking coefficient. The constructed sealing deposition model is quite similar to the characterized LTO sealing deposition found in the literature [39].

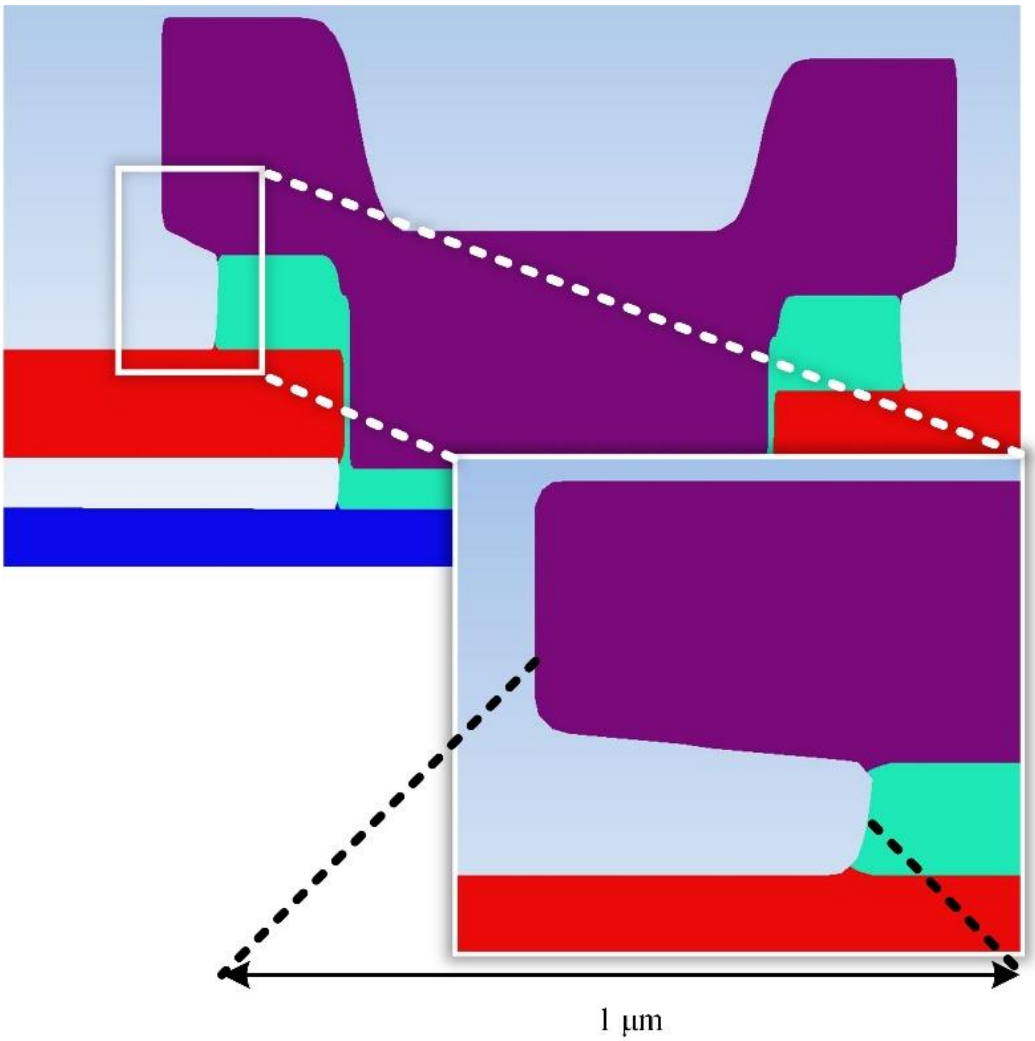


Figure 3.25. The virtualized structure after oxide removal in BHF (Step-33).

The under etch of oxide underneath the photoresist was investigated and it is observed that the oxide which seals the cavities remains without any failure as depicted in Figure 3.25. Considering the selectivity over photoresist, which is pre-defined by the simulation program for oxide removal as 0.1, the 1 µm oxide is under etched during 1.2 µm oxide removal in BHF.

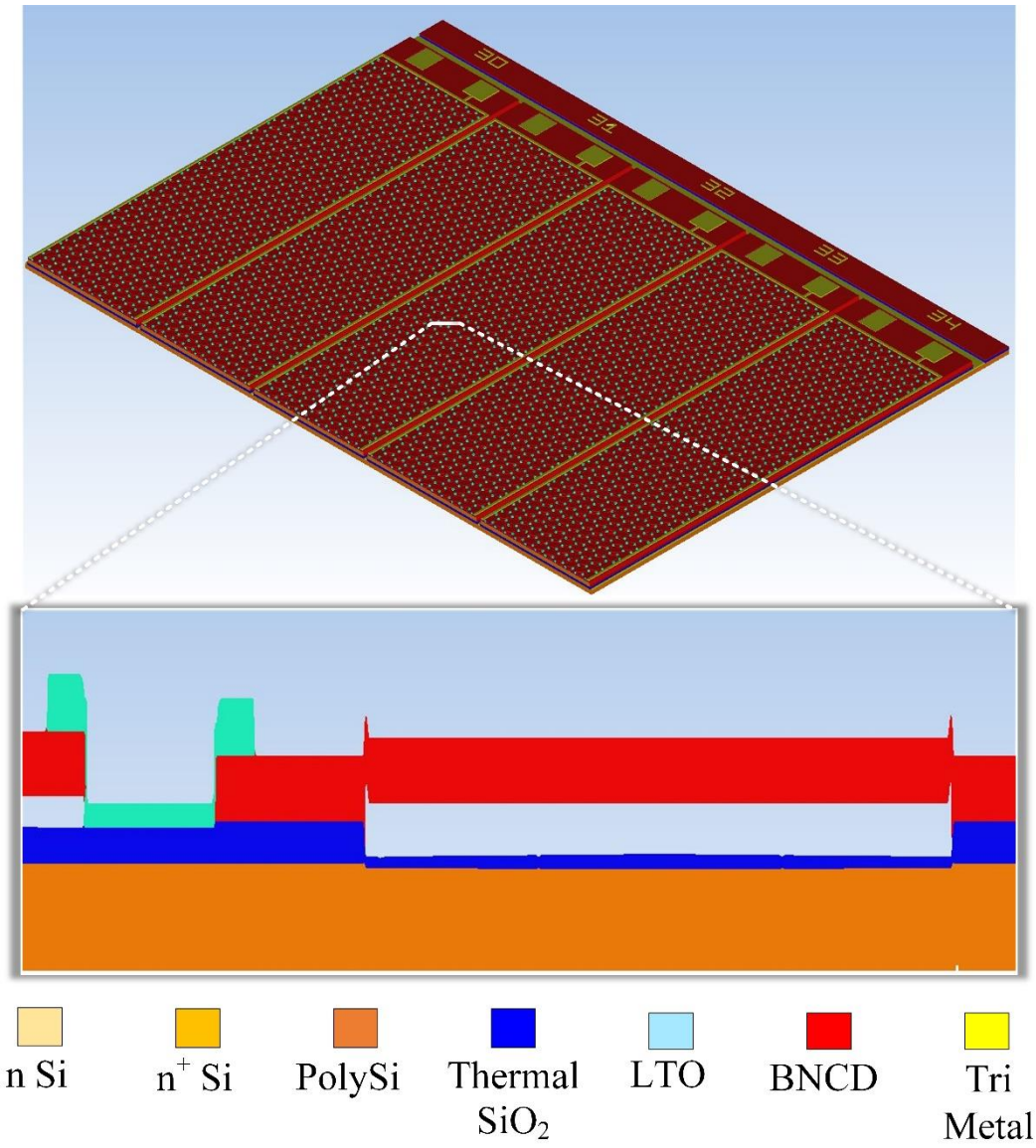


Figure 3.26. The partial view of final constructed structure.

3.4.2 Process Analysis on Sentaurus

Another virtual microfabrication tool that the developed microfabrication can be virtually analyzed and verified is the commercially available Sentaurus TCAD (Synopsys, California, USA). Sentaurus provides realistic electrical, thermal, optical and visual characterization and analysis of silicon-based and compound semiconductor devices. The topography tool of Sentaurus is advantageous for a

realistic investigation of the microfabrication since the topography tool enables to define the processing machines (deposition, RIE, etc…) and their properties. Therefore Sentaurus and its topography tool was used for constructing a realistic model of the developed microfabrication in another environment other than Semulator3D and virtually examining it.

In the Sentaurus, doping profile of the handle wafer of the SOI wafer before and after the BOX layer were constructed on a 2-D model. As mentioned above the SOI wafer used in the developed microfabrication was a special wafer having a conductive handle wafer at its surface (0.005 Ω.cm).

The modeling of the developed microfabrication in Sentaurus was realized on a silicon wafer that has the properties of the device layer of SOI wafer (0.005 Ω.cm, P doped, 2 μm). Considering the computational complexity and time, 2-D modeling of a single CMUT cell with an etch channel and hole next to cell was performed. Diamond deposition and the afterwards process steps were not modeled in Sentaurus, since diamond is not a defined material in the database of the simulation program. Therefore, in addition to modeling of handle wafer, processing of CMUT cell starting from the thermal oxidation step (Step-6), to the patterning of the second sacrificial polysilicon layer step (Step-21) was modeled in Sentaurus.

According to the resistivity formula of a silicon sample given in the Eq. 3.1, where N_D is the dopant concentration, q is the charge of one electron (1.6×10^{-19} C) and μ_n is the electron mobility in the silicon sample (1200 cm^2/V-s), given the resistivity, the doping concentration of a silicon sample can be found.

$$\rho = \frac{1}{q\, N_D \mu_n} \tag{3.1}$$

The bulk resistivity of the handle wafer of the SOI wafer is 5 Ω-cm. Therefore, using the Eq. 3.1 an initial wafer that has the initial dopant (Phosphorus) concentration of 1.0×10^{15} cm^{-3} was constructed. Afterwards, the doping of the wafer with Phosphorus was modeled (dose = 1.0×10^{15} cm^{-2}, Energy = 80 KeV). Then, the annealing was modeled in which the wafer was waited under 1050°C for 60 minutes. Finally, the

BOX layer was constructed on handle wafer by wet oxidation at 1000°C for 300 minutes.

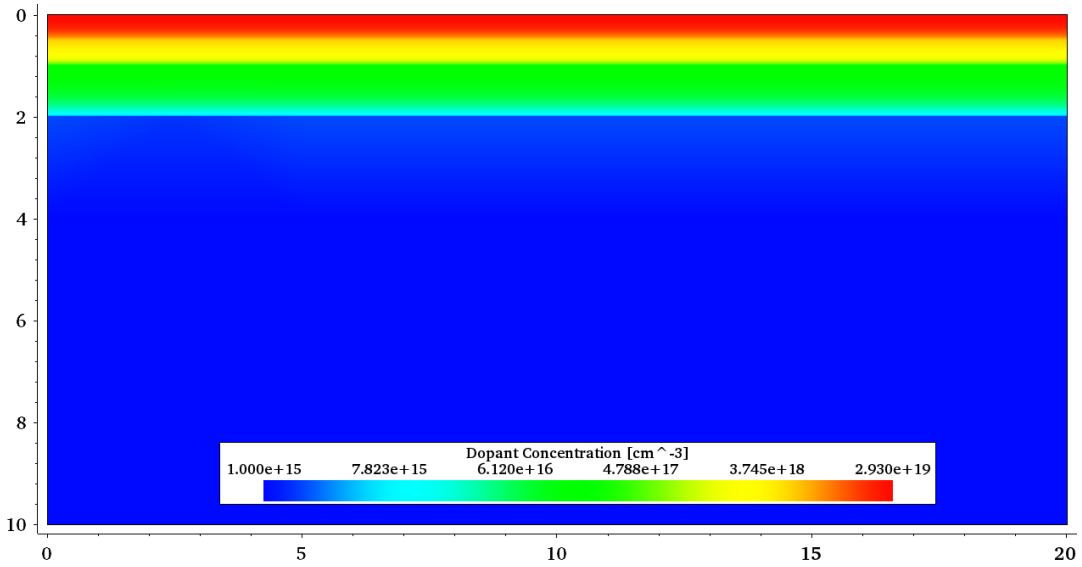


Figure 3.27. The doping profile of the handle wafer before the BOX layer is constructed.

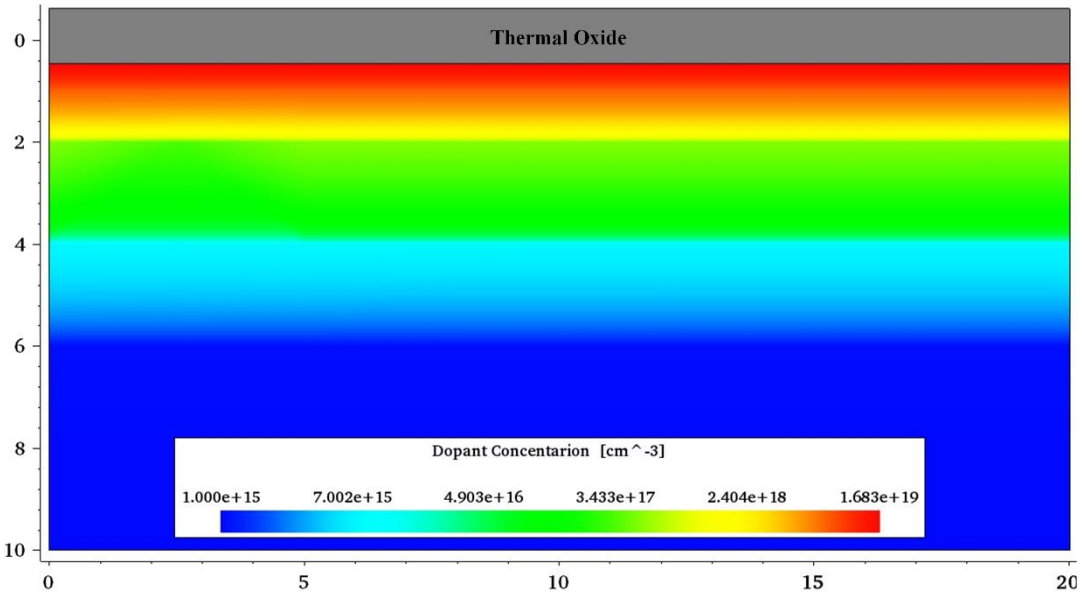


Figure 3.28. The doping profile of the handle wafer after the BOX layer is constructed.

As seen from Figures 3.27 and Figure 3.28, after the oxidation, the highest dopant concentration at the surface of the silicon sample decreases from $2.930x10^{19}$ cm^{-3} to $1.683x10^{19}$ cm^{-3} where the decline in the surface dopant concentration was expected. On the other hand, since during the oxidation more of the dopants move into silicon sample the depth of high conductive surface that has a dopant concentration higher than $1.0x10^{19}$ cm^{-3} (red area) has increased from 0.5 μm to 1 μm. Furthermore, the total depth of the conductive surface that has a dopant concentration greater than $2.0x10^{1}$ cm^{-16} (green area) has increased from 2 μm to 3.5 μm.

The modeling of the fabrication of a CMUT cell has started with the definition of the initial wafer. Using the Eq. 3.1, an initial wafer that has the same properties as the device layer (0.005 Ω-cm, P) and initial dopant (Phosphorus) concentration of $1.0x10^{18}$ cm^{-3} was constructed. Then, the RIE and deposition machines were defined using the topography tool. In contrary, during modeling of the microfabrication in Semulator3D, the etch rates and selectivity of the RIE machines were defined according to the literature [98, 99]. However, in reality those values would be depending on the machine properties found in the facility where the microfabrication was realized. The etching times was determined to etch 10 to 20 % more than the thickness of the layer that is being patterned. The Polysilicon deposition machine was modeled as LPCVD furnace, providing a conformal deposition. Afterwards the machine definitions, the modeling of the fabrication of CMUT cell through the process steps 6 to 21 of the developed process flow was performed in Sentaurus. For the modeling of the thermal oxidations, the recipe specified in the process flow was used.

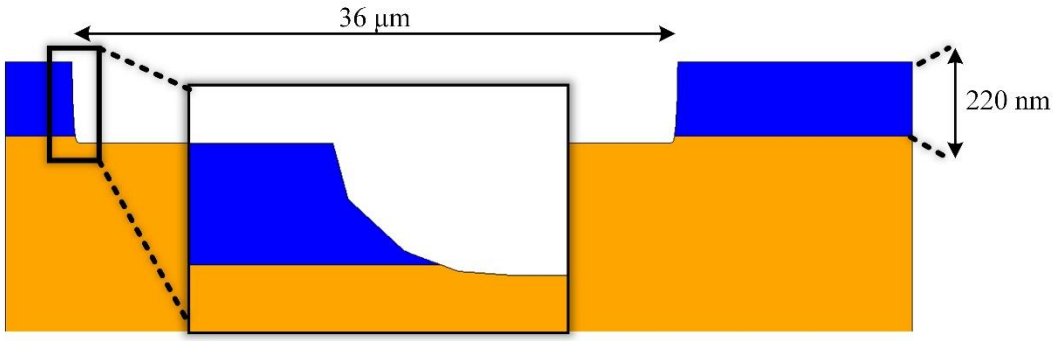


Figure 3.29. 2-D cross sectional view of the structure after the thermal oxide is patterned constructed in Sentaurus (Step-10).

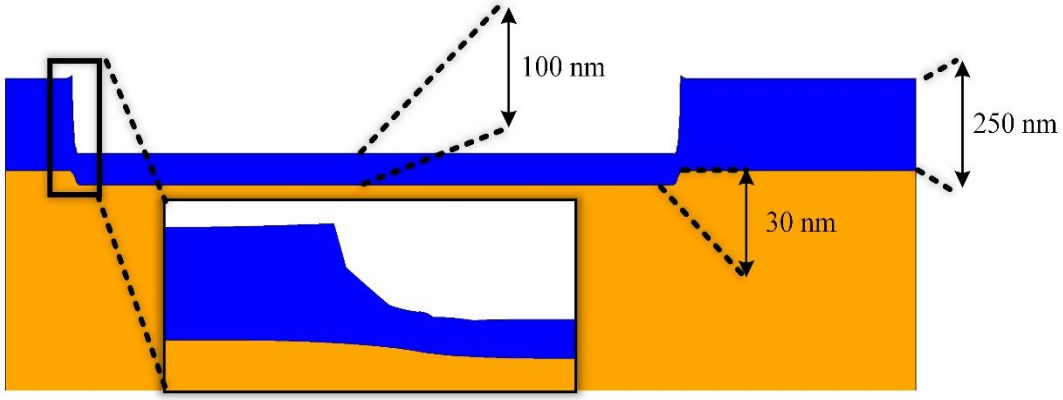


Figure 3.30. 2-D cross sectional view of the structure after the second thermal oxidation constructed in Sentaurus (Step-11).

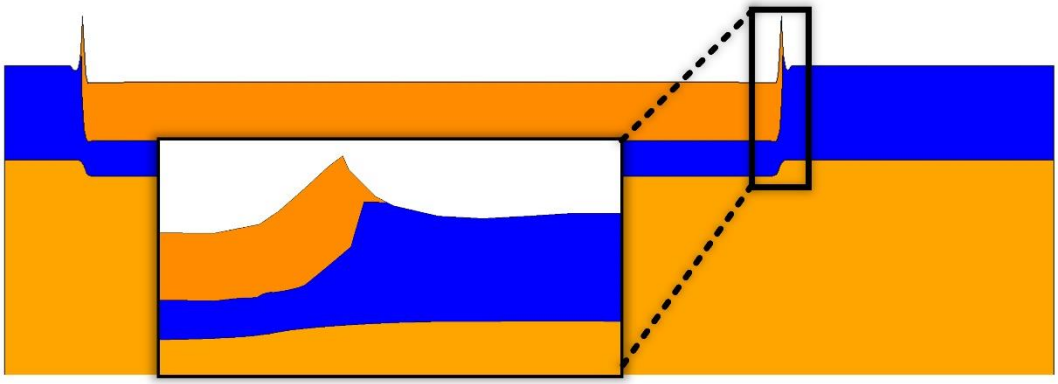


Figure 3.31. 2-D cross sectional view of the structure after the patterning of the Poly1 layer constructed in Sentaurus (Step-16).

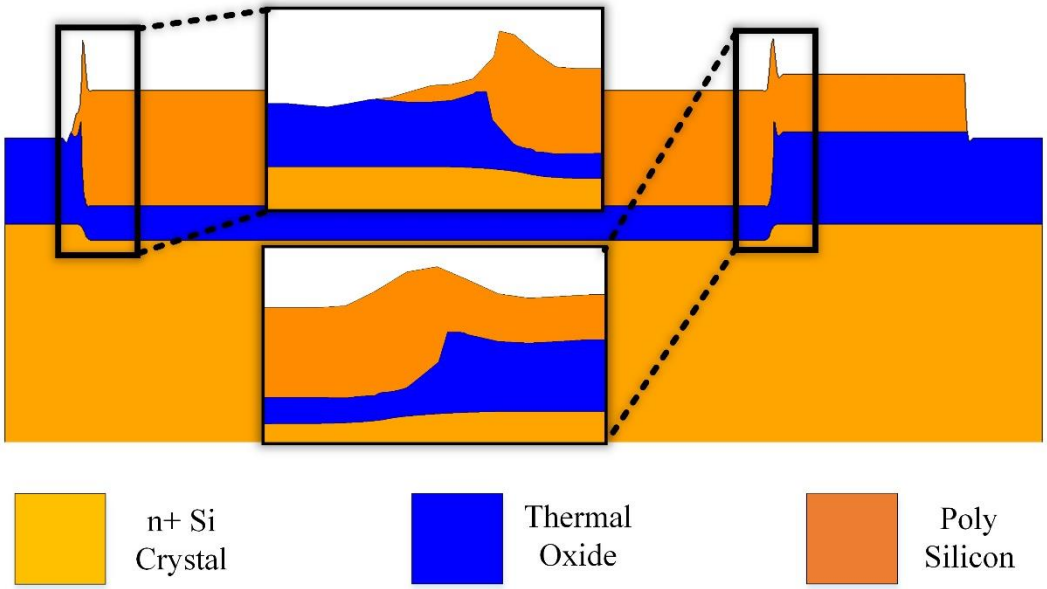


Figure 3.32. 2-D cross sectional view of the structure after the patterning of the Poly2 layer constructed in Sentaurus (Step-21).

Based on the visualization of the structures built through Semulator3D and Sentaurus, it has been observed that similar structures were constructed so that the feasibility of the developed microfabrication was confirmed.

CHAPTER 4

FARADAY CAGED CMUT AND A TRANSMIT AND RECEIVE OPERATION

In this chapter, a novel Faraday caged CMUT array and a new transmit and receive operation are introduced. As observed through the FEM simulations, the benefit of the Faraday caged CMUT array and the transmit and receive operation compared to a CMUT array fabricated through the developed microfabrication is the reduction in the electrical crosstalk and parasitic capacitance during the transmit and receive operations, respectively.

4.1 The Faraday Caged CMUT Array

The Faraday caged CMUT array includes an individual electrically addressable conductive shield for each array element that behaves as a Faraday Cage. It is placed underneath the bottom electrode, which the DC and AC signal for CMUT operation are applied [79]. The individual third terminal for the array element provides the control over the state of this individual third electrode whether it is floating or grounded. The representative cross-sectional view for a Faraday caged CMUT array is as given in Figure 4.1.

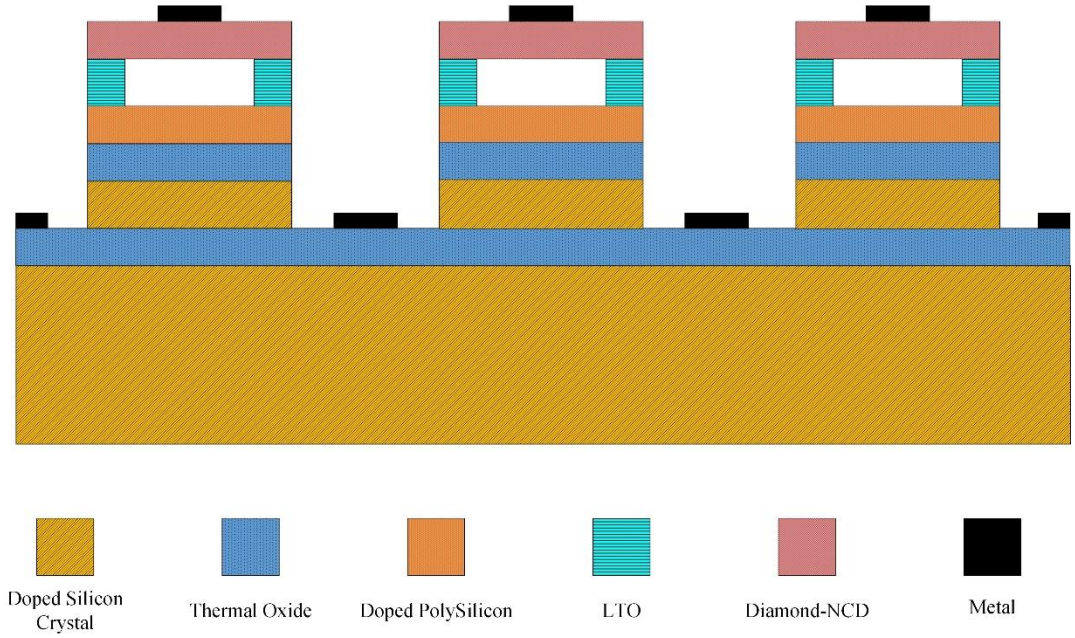


Figure 4.1. The representative cross-sectional view of a Faraday caged CMUT array.

Figure 4.1 shows a representative structure for Faraday caged CMUT array in which the structure involves three neighboring elements with a metal isolation line passing through between the elements. Each array element consists of a diamond membrane with a metal top electrode on top of it. Underneath the membrane, there is an anchor layer, which is made of a dielectric material such as silicon dioxide, and it provides the mechanical support to moveable membrane and isolates it from the polysilicon bottom electrode. So, a conductive material such as doped polysilicon can be used as the bottom electrode for the CMUT array where the biasing and signal voltage are applied to bottom electrode and the top electrode is grounded [79].

The parasitic capacitance is the additional constant capacitance to the signal to ground capacitance of a CMUT array element. The coupling capacitance is the capacitance between two neighboring array elements. The electrical crosstalk is the coupling of the electromagnetic waves of a CMUT array element to another element. The neighboring array element would affect the parasitic capacitance, the coupling capacitance, and the electrical crosstalk through the silicon substrate. Thus, placing an individual Faraday cage underneath the CMUT array element would suppress the

effects coming through the silicon substrate significantly. Therefore, as it is seen in Figure 4.1, for each array element, underneath the polysilicon bottom electrode there is an individual conductive Faraday cage constructed from the device layer of an SOI wafer that is doped silicon. The bottom electrode and the Faraday cage are isolated through a dielectric layer, such as thermal oxide, whereas each Faraday cage of a CMUT array element is separated from the other and substrate through a thermal oxide layer.

Furthermore, the Faraday cage of an individual CMUT array element is electrically controlled through an individual third terminal of that element so that, the Faraday Cage can be grounded or floating [79].

4.2 Parasitic Capacitance and Electrical Crosstalk Calculations

Electrical effect of the Faraday cage on the parasitic capacitance, coupling capacitance and the electrical crosstalk were examined through the FEM simulations performed using the Semulator3D and Agilent Advanced Design System (ADS, Keysight Technologies, California, USA) and Electro Magnetic Professional (EMPro, Keysight Technologies, California, USA).

Semulator3D has a powerful tool for extracting capacitance between each existing conductor in 3-D environment whereas ADS and EMPro work harmonically to perform electrical analysis of a 3-D built structure. In Semulator3D, a 3-D structure is built voxel by voxel through the defined process flow and layout. After that, the capacitance matrix that includes capacitance between each node is constructed using the capacitance segmentation feature in Semulator3D that provides the ability to accurately calculate the cross-capacitance values between each conductor existing in the voxel by voxel constructed 3-D structure. In ADS, 3-D a structure is built through a defined substrate technology and layout and then FEM model are constructed whereas in EMPro the electromagnetic analysis of the constructed FEM structure is performed.

To observe the electrical advantage of the Faraday cage, two 2-element 1-D CMUT arrays were examined. One array was representing a CMUT array structure without a Faraday cage and therefore representing a CMUT array structure that would be fabricated through the proposed microfabrication or a similar microfabrication to the proposed one whereas the other CMUT array was representing a Faraday caged CMUT array as given in Figure 4.1.

The CMUT cell orientation for a 1-D M-element CMUT array is depicted in Figure 4.2., wherein the CMUT array elements are shown with circles. The row number of the CMUT array determines the array height where a single row includes three CMUT cells in which, a CMUT cell can belong to only one row as shown in Figure 4.2. This is a representative figure for 1-D CMUT array that is valid for regular and Faraday caged CMUT arrays and was used as a base for the structures built in the computer environment. Some dimensions have been marked on Figure 4.2; where d_{C2C} is the cell to cell distance between CMUT cells, r_{mem} is the radius of the circular shaped CMUT cells, d_{A2A} is the element to element distance of CMUT arrays, and w_A is the element width of the CMUT arrays.

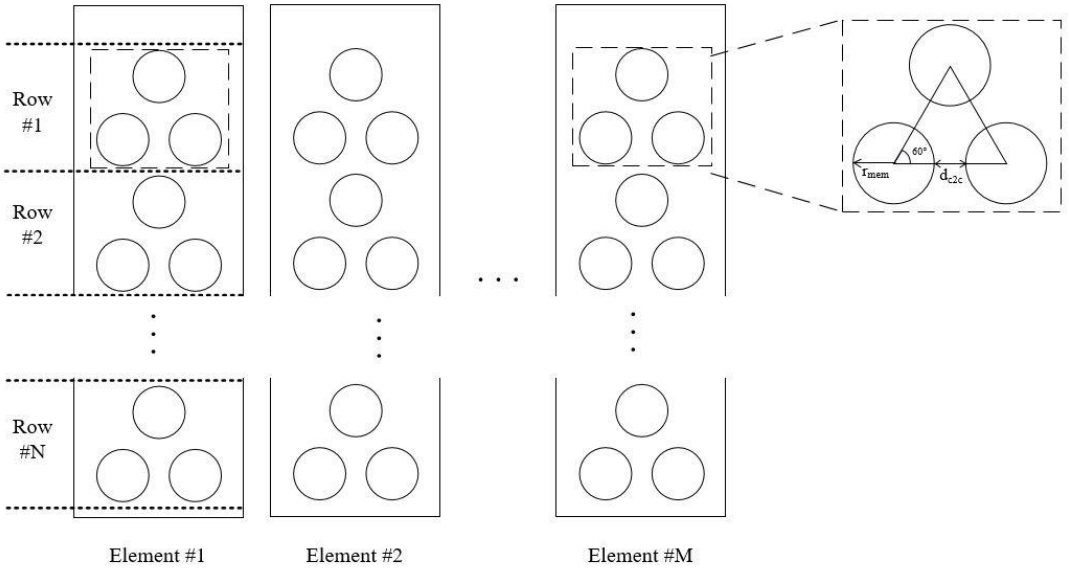


Figure 4.2. CMUT cell orientation for a 1-D M-element CMUT array.

The basis representative cross-sectional views of 2-element 1-D regular CMUT array (a) and 2-element 1-D Faraday caged CMUT array (b) built in the computer environment for electrical analysis are as shown in Figure 4.3. Some dimensions have been marked on the regular CMUT array as shown in Figure 4.3.(a) where; t_{subs} is the substrate thickness, t_{BOX} is the dielectric layer thickness, t_{bottom} is the bottom electrode, t_{ins} is the insulator layer thickness, t_{gap} is the cavity gap of the CMUT cell, t_{etc} is the etch channel thickness, t_{mem} is the membrane thickness, t_{metal} is the metal thickness, r_e is the radius of the circular shaped top electrode of the CMUT cell, w_{iso} is the width of the isolation line**,** and d_{etc} is the diameter of the circular shaped etch via. In addition to marked dimensions on regular CMUT array structure, some dimensions have been marked on the Faraday caged CMUT array as depicted in Figure 4.3 (b). where; $t_{Faraday}$ is the thickness of the Faraday Cage, t_{therox} is the thickness of the thermally grown silicon dioxide layer standing on top of the Faraday cage and $d_{Faraday2A}$ is the distance of Faraday cage border to the bottom electrode border.

In Semulator3D, the capacitance analysis can be performed in DC, and therefore, the resistivity of the CMUT structure is not taken into account. However, for the simulation performed in the ADS&EMPro the structure was examined over a frequency range taking the resistivity of the CMUT structure into account.

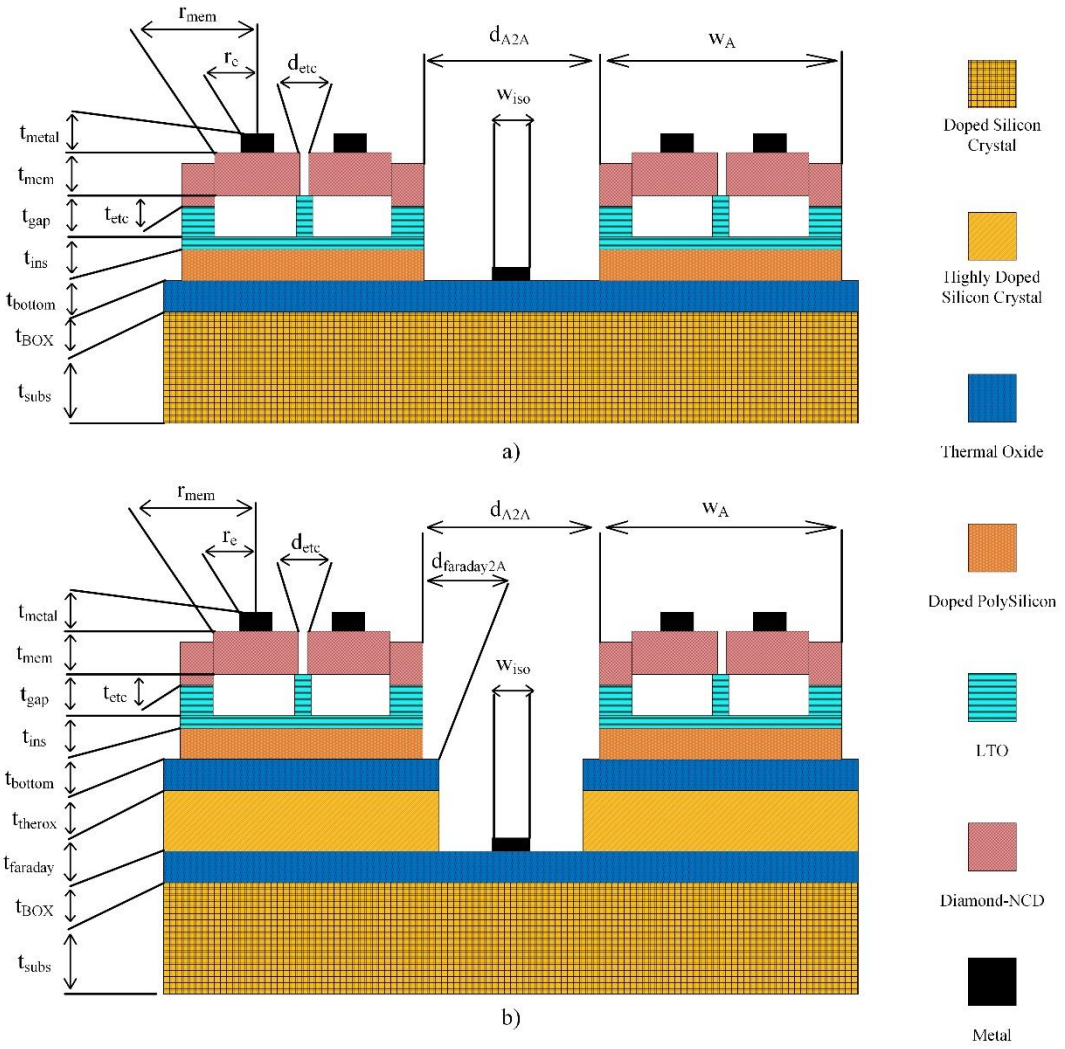


Figure 4.3. The basis representative cross-sectional views of 2-element 1-D regular CMUT array (a) and 2-element 1-D Faraday caged CMUT array (b) built in the computer environment.

Table 4.1 and 4.2 show the dimension parameter values and material properties of the CMUT arrays built for electrical analysis in Semulator3D and ADS&EMPro, respectively. Semulator3D lets users define a material as conductor and dielectric only, whereas, in ADS and EMPro, a material can be defined as conductor, semiconductor, and dielectric. Thus, the material definitions in these programs were slightly different from each other. This slight difference did not significantly affect the simulation results.

Table 4.1. Dimension parameter values of the structures built for regular and Faraday caged CMUT arrays in computer environment.

Dimension parameter	**Value (µm)**
t_{subs}	400
t_{BOX}	1
$t_{Faraday}$	2
t_{therox}	1
t_{bottom}	1
t_{ins}	0.15
t_{gap}	1.1
t_{etc}	0.25
t_{mem}	1
t_{metal}	0.5
r_{mem}	18
r_e	9
d_{etc}	4
d_{C2C}	7.3
$d_{Faraday2A}$	2
d_{A2A}	24
w_A	116
w_{iso}	10

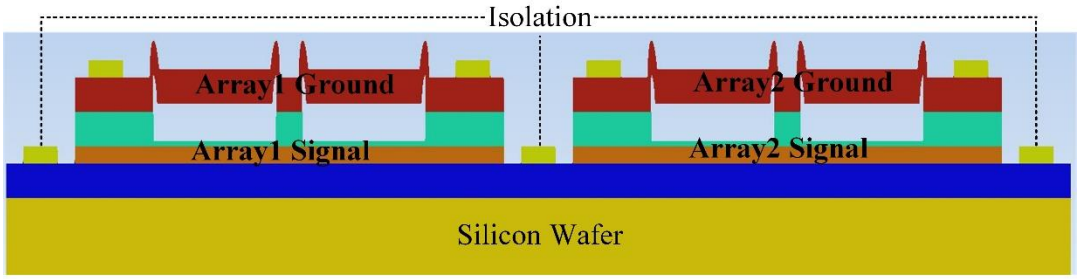
Table 4.2. Material definition and properties of the structures built for regular and Faraday caged CMUT arrays in computer environment.

Material		Type	Conductivity (Siemens/m)	Dielectric Constant
Gold		Conductor	$4.1x10^7$	-
PolySilicon		Conductor	$5.0x10^4$	-
LTO		Dielectric	-	4.3
Thermal Silicon Dioxide		Dielectric	-	3.9
BNCD	Semulator3D	Conductor	$5.0x10^3$	-
	ADS&EMPro	Semicond.	$5.0x10^3$	5.5
Highly Doped Si	Semulator3D	Conductor	$2.0x10^4$	-
	ADS&EMPro	Semicond.	$2.0x10^4$	11.9
Doped Si	Semulator3D	Conductor	20	-
	ADS&EMPro	Semicond.	20	11.9

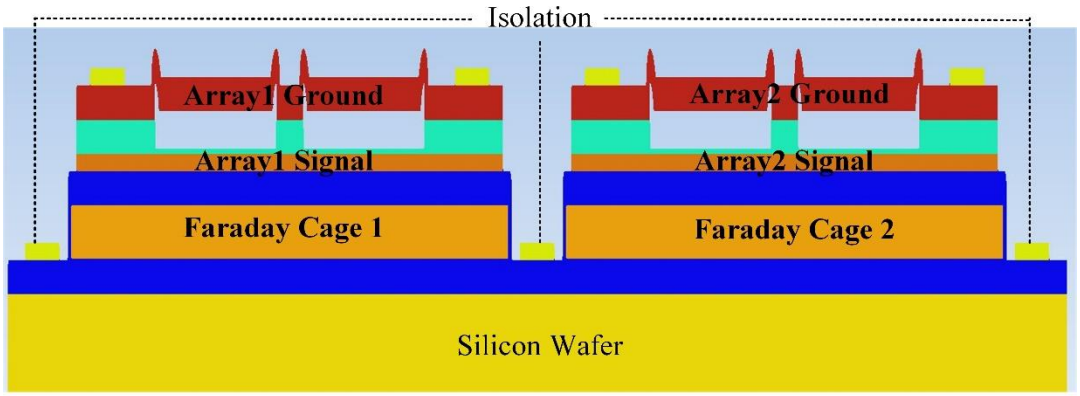
Semulator3D was used for virtual microfabrication of the structures representing regular and Faraday caged CMUT arrays as depicted in Figure 4.3, with the given thickness parameters in Table 4.1. For this purpose, microfabrication process flows for regular and Faraday caged CMUT arrays were defined. In accordance with the defined process flows, proper layouts for regular and Faraday caged CMUT arrays with row number values of 1,2 and 3 were defined with the parameter values given in Table 4.1. Then the capacitances were extracted between each node found in the 2-element regular and Faraday caged CMUT arrays when row number is one, two, and three.

The 2-element regular CMUT array contains 6 nodes which are, the bottom electrode of the first array element (Array1 Signal, “A1”), the top electrode of the first array element (Array1 Ground, “G1”), the bottom electrode of the second array element (Array2 Signal, “A2”), the top electrode of the second array element (Array 2 Ground, “G2”), the isolation line (Isolation, “ISO”) and the substrate (Silicon Wafer, “SW”).

The 2-element Faraday caged CMUT array contains 8 nodes which are, the bottom electrode of the first array element (Array1 Signal, “A1”), the top electrode of the first array element (Array1 Ground, “G1”), the Faraday cage of the first array element (Array 1 Faraday Cage, “FC1”), the bottom electrode of the second array element (Array2 Signal, “A2”), the top electrode of the second array element (Array 2 Ground, “G2”), the Faraday cage of the second array element (Array 2 Faraday Cage, “FC2”), the isolation line (Isolation, “ISO”) and the substrate (Silicon Wafer, “SW”). The cross-sectional views of constructed structures and the corresponding nodes on the structures representing regular and Faraday caged CMUT arrays in Semulator3D are as given in Figure 4.4.



a)



b)

Figure 4.4. Cross-sectional view of constructed structures representing regular (a) and Faraday caged (b) CMUT arrays in Semulator3D.

The capacitance matrixes that include the capacitances between each node of the 2-element regular CMUT array when row number is one, two, and three are given in Tables 4.3-4.5, respectively.

Table 4.3. Capacitance matrix of the regular CMUT array when row number is 1.

Node Names	Array1 Signal (pF)	Array1 Ground (pF)	Array2 Signal (pF)	Array2 Ground (pF)	Isolation (pF)	Silicon Wafer (pF)
Array1 Signal		$6.81x10^{-1}$	$5.62x10^{-8}$	$4.54x10^{-7}$	$2.81x10^{-4}$	$7.45x10^{-1}$
Array1 Ground	$6.81x10^{-1}$		$4.49x10^{-7}$	$3.61x10^{-6}$	$1.67x10^{-3}$	$3.39x10^{-3}$
Array2 Signal	$5.62x10^{-8}$	$4.49x10^{-7}$		$6.81x10^{-1}$	$2.80x10^{-4}$	$7.45x10^{-1}$
Array2 Ground	$4.54x10^{-7}$	$3.61x10^{-6}$	$6.81x10^{-1}$		$1.67x10^{-3}$	$3.40x10^{-3}$
Isolation	$2.81x10^{-4}$	$1.67x10^{-3}$	$2.80x10^{-4}$	$1.67x10^{-3}$		$4.47x10^{-1}$
Silicon Wafer	$7.45x10^{-1}$	$3.39x10^{-3}$	$7.45x10^{-1}$	$3.40x10^{-3}$	$4.47x10^{-1}$	

Table 4.4. Capacitance matrix of the regular CMUT array when row number is 2.

Node Names	Array1 Signal (pF)	Array1 Ground (pF)	Array2 Signal (pF)	Array2 Ground (pF)	Isolation (pF)	Silicon Wafer (pF)
Array1 Signal		$9.42x10^{-1}$	$8.13x10^{-8}$	$6.57x10^{-7}$	$3.50x10^{-4}$	1.07
Array1 Ground	$9.42x10^{-1}$		$6.53x10^{-7}$	$5.21x10^{-6}$	$2.08x10^{-3}$	$4.25x10^{-3}$
Array2 Signal	$8.13x10^{-8}$	$6.53x10^{-7}$		$9.42x10^{-1}$	$3.49x10^{-4}$	1.07
Array2 Ground	$6.57x10^{-7}$	$5.21x10^{-6}$	$9.42x10^{-1}$		$2.08x10^{-3}$	$4.26x10^{-3}$
Isolation	$3.50x10^{-4}$	$2.08x10^{-3}$	$3.49x10^{-4}$	$2.08x10^{-3}$		$5.36x10^{-1}$
Silicon Wafer	1.07	$4.25x10^{-3}$	1.07	$4.26x10^{-3}$	$5.36x10^{-1}$	

Table 4.5. Capacitance matrix of the regular CMUT array when row number is 3.

Node Names	Array1 Signal (pF)	Array1 Ground (pF)	Array2 Signal (pF)	Array2 Ground (pF)	Isolation (pF)	Silicon Wafer (pF)
Array1 Signal		1.20	$1.06x10^{-7}$	$8.57x10^{-7}$	$4.20x10^{-4}$	1.40
Array1 Ground	1.20		$8.50x10^{-7}$	$6.85x10^{-6}$	$2.50x10^{-3}$	$5.10x10^{-3}$
Array2 Signal	$1.06x10^{-7}$	$8.50x10^{-7}$		1.20	$4.19x10^{-4}$	1.40
Array2 Ground	$8.57x10^{-7}$	$6.85x10^{-6}$	1.20		$2.50x10^{-3}$	$5.11x10^{-3}$
Isolation	$4.20x10^{-4}$	$2.50x10^{-3}$	$4.19x10^{-4}$	$2.50x10^{-3}$		$6.24x10^{-1}$
Silicon Wafer	1.40	$5.10x10^{-3}$	1.40	$5.11x10^{-3}$	$6.24x10^{-1}$	

The capacitance matrixes that include the capacitances between each node of the 2-element regular CMUT array when row number is one, two, and three are given in Tables 4.6-4.8, respectively.

Table 4.6. Capacitance matrix of the Faraday caged CMUT array when row number is 1.

Node Names	Array1 Signal (pF)	Array1 Ground (pF)	Array2 Signal (pF)	Array2 Ground (pF)
Array1 Signal		$6.81x10^{-1}$	$5.79x10^{-7}$	$3.25x10^{-6}$
Array1 Ground	$6.81x10^{-1}$		$3.21x10^{-6}$	$1.80x10^{-5}$
Array2 Signal	$5.79x10^{-7}$	$3.21x10^{-6}$		$6.81x10^{-1}$
Array2 Ground	$3.25x10^{-6}$	$1.80x10^{-5}$	$6.81x10^{-1}$	
Array1 Faraday Cage	$7.45x10^{-1}$	$2.88x10^{-3}$	$3.18x10^{-6}$	$1.78x10^{-5}$
Array2 Faraday Cage	$3.21x10^{-6}$	$1.78x10^{-5}$	$7.45x10^{-1}$	$2.89x10^{-3}$
Isolation	$3.39x10^{-4}$	$1.39x10^{-3}$	$3.38x10^{-4}$	$1.39x10^{-3}$
Silicon Wafer	$1.78x10^{-4}$	$3.52x10^{-4}$	$1.77x10^{-4}$	$3.53x10^{-4}$

Table 4.6. (Continued)

Node Names	Array1 Faraday Cage (pF)	Array2 Faraday Cage (pF)	Isolation (pF)	Silicon Wafer (pF)
Array1 Signal	$7.45x10^{-1}$	$3.21x10^{-6}$	$3.39x10^{-4}$	$1.78x10^{-4}$
Array1 Ground	$2.88x10^{-3}$	$1.78x10^{-5}$	$1.39x10^{-3}$	$3.52x10^{-4}$
Array2 Signal	$3.18x10^{-6}$	$7.45x10^{-1}$	$3.38x10^{-4}$	$1.77x10^{-4}$
Array2 Ground	$1.78x10^{-5}$	$2.89x10^{-3}$	$1.39x10^{-3}$	$3.53x10^{-4}$
Array1 Faraday Cage		$1.78x10^{-5}$	$3.36x10^{-3}$	$7.56x10^{-1}$
Array2 Faraday Cage	$1.78x10^{-5}$		$3.36x10^{-3}$	$7.56x10^{-1}$
Isolation	$3.36x10^{-3}$	$3.36x10^{-3}$		$4.44x10^{-1}$
Silicon Wafer	$7.56x10^{-1}$	$7.56x10^{-1}$	$4.44x10^{-1}$	

Table 4.7. Capacitance matrix of the Faraday caged CMUT array when row number is 2.

Node Names	Array1 Signal (pF)	Array1 Ground (pF)	Array2 Signal (pF)	Array2 Ground (pF)
Array1 Signal		$9.42x10^{-1}$	$8.37x10^{-7}$	$4.68x10^{-6}$
Array1 Ground	$9.42x10^{-1}$		$4.61x10^{-6}$	$2.60x10^{-5}$
Array2 Signal	$8.37x10^{-7}$	$4.61x10^{-6}$		$9.42x10^{-1}$
Array2 Ground	$4.68x10^{-6}$	$2.60x10^{-5}$	$9.42x10^{-1}$	
Array1 Faraday Cage	1.07	$3.61x10^{-3}$	$4.58x10^{-6}$	$2.56x10^{-5}$
Array2 Faraday Cage	$4.62x10^{-6}$	$2.55x10^{-5}$	1.07	$3.62x10^{-3}$
Isolation	$4.23x10^{-4}$	$1.73x10^{-3}$	$4.21x10^{-4}$	$1.74x10^{-3}$
Silicon Wafer	$2.22x10^{-4}$	$4.36x10^{-4}$	$2.21x10^{-4}$	$4.37x10^{-4}$

Table 4.7. (Continued)

Node Names	Array1 Faraday Cage (pF)	Array2 Faraday Cage (pF)	Isolation (pF)	Silicon Wafer (pF)
Array1 Signal	1.07	$4.62x10^{-6}$	$4.23x10^{-4}$	$2.22x10^{-4}$
Array1 Ground	$3.61x10^{-3}$	$2.55x10^{-5}$	$1.73x10^{-3}$	$4.36x10^{-4}$
Array2 Signal	$4.58x10^{-6}$	1.07	$4.21x10^{-4}$	$2.21x10^{-4}$
Array2 Ground	$2.56x10^{-5}$	$3.62x10^{-3}$	$1.74x10^{-3}$	$4.37x10^{-4}$
Array1 Faraday Cage		$2.54x10^{-5}$	$4.17x10^{-3}$	1.08
Array2 Faraday Cage	$2.54x10^{-5}$		$4.18x10^{-3}$	1.08
Isolation	$4.17x10^{-3}$	$4.18x10^{-3}$		$5.32x10^{-1}$
Silicon Wafer	1.08	1.08	$5.32x10^{-1}$	

Table 4.8. Capacitance matrix of the Faraday caged CMUT array when row number is 3.

Node Names	Array1 Signal (pF)	Array1 Ground (pF)	Array2 Signal (pF)	Array2 Ground (pF)
Array1 Signal		1.20	$1.09x10^{-6}$	$6.15x10^{-6}$
Array1 Ground	1.20		$6.06x10^{-6}$	$3.40x10^{-5}$
Array2 Signal	$1.09x10^{-6}$	$6.06x10^{-6}$		1.20
Array2 Ground	$6.15x10^{-6}$	$3.40x10^{-5}$	1.20	
Array1 Faraday Cage	1.40	$4.34x10^{-3}$	$5.97x10^{-6}$	$3.34x10^{-5}$
Array2 Faraday Cage	$6.02x10^{-6}$	$3.33x10^{-5}$	1.40	$4.35x10^{-3}$
Isolation	$5.07x10^{-4}$	$2.08x10^{-3}$	$5.04x10^{-4}$	$2.08x10^{-3}$
Silicon Wafer	$2.66x10^{-4}$	$5.19x10^{-4}$	$2.65x10^{-4}$	$5.20x10^{-4}$

Table 4.8. (Continued)

Node Names	Array1 Faraday Cage (pF)	Array2 Faraday Cage (pF)	Isolation (pF)	Silicon Wafer (pF)
Array1 Signal	1.40	$6.02x10^{-6}$	$5.07x10^{-4}$	$2.66x10^{-4}$
Array1 Ground	$4.34x10^{-3}$	$3.33x10^{-5}$	$2.08x10^{-3}$	$5.19x10^{-4}$
Array2 Signal	$5.97x10^{-6}$	1.40	$5.04x10^{-4}$	$2.65x10^{-4}$
Array2 Ground	$3.34x10^{-5}$	$4.35x10^{-3}$	$2.08x10^{-3}$	$5.20x10^{-4}$
Array1 Faraday Cage		$3.30x10^{-5}$	$4.99x10^{-3}$	1.40
Array2 Faraday Cage	$3.30x10^{-5}$		$4.99x10^{-3}$	1.40
Isolation	$4.99x10^{-3}$	$4.99x10^{-3}$		$6.19x10^{-1}$
Silicon Wafer	1.40	1.40	$6.19x10^{-1}$	

To overcome the computational complexity in Semulator3D, for the extraction of the capacitance matrix of the structures with high row number, the linearity of the capacitances existing in the capacitance matrix for regular and Faraday caged CMUT arrays were examined. As it is verified from the Tables 4.3 to 4.8 that all of the capacitances found in 2-element regular and Faraday caged CMUT arrays are linear with the row number. Thus, it is possible to extrapolate the capacitance matrix of regular and Faraday caged CMUT arrays for high row number cases. The capacitance matrix of regular and Faraday caged CMUT arrays when the row number is 10 were extrapolated as given in Table 4.9 and Table 4.10, respectively.

Table 4.9. Extrapolated capacitance matrix of the regular CMUT array when the row number is 10.

Node Names	Array1 Signal (pF)	Array1 Ground (pF)	Array2 Signal (pF)	Array2 Ground (pF)	Isolation (pF)	Silicon Wafer (pF)
Array1 Signal		3.03	$2.82\text{x}10^{-7}$	$2.28\text{x}10^{-6}$	$9.08\text{x}10^{-4}$	3.68
Array1 Ground	3.03		$2.28\text{x}10^{-6}$	$1.80\text{x}10^{-5}$	$5.41\text{x}10^{-3}$	$1.11\text{x}10^{-2}$
Array2 Signal	$2.82\text{x}10^{-7}$	$2.28\text{x}10^{-6}$		3.03	$9.04\text{x}10^{-4}$	3.68
Array2 Ground	$2.28\text{x}10^{-6}$	$1.80\text{x}10^{-5}$	3.03		$5.42\text{x}10^{-3}$	$1.11\text{x}10^{-2}$
Isolation	$9.08\text{x}10^{-4}$	$5.41\text{x}10^{-3}$	$9.04\text{x}10^{-4}$	$5.42\text{x}10^{-3}$		1.24
Silicon Wafer	3.68	$1.11\text{x}10^{-2}$	3.68	$1.11\text{x}10^{-2}$	1.24	

Table 4.10. Extrapolated capacitance matrix of the Faraday caged CMUT array when the row number is 10.

Node Names	Array1 Signal (pF)	Array1 Ground (pF)	Array2 Signal (pF)	Array2 Ground (pF)
Array1 Signal		3.03	$2.90x10^{-6}$	$1.61x10^{-5}$
Array1 Ground	3.03		$1.59x10^{-5}$	$8.97x10^{-5}$
Array2 Signal	$2.90x10^{-6}$	$1.59x10^{-5}$		3.03
Array2 Ground	$1.61x10^{-5}$	$8.97x10^{-5}$	3.03	
Array1 Faraday Cage	3.67	$9.44x10^{-3}$	$1.57x10^{-5}$	$8.79x10^{-5}$
Array2 Faraday Cage	$1.59x10^{-5}$	$8.76x10^{-5}$	3.67	$9.47x10^{-3}$
Isolation	$1.09x10^{-3}$	$4.48x10^{-3}$	$1.08x10^{-3}$	$4.48x10^{-3}$
Silicon Wafer	$5.74x10^{-4}$	$1.10x10^{-3}$	$5.70x10^{-4}$	$1.10x10^{-3}$

Table 4.10. (Continued)

Node Names	Array1 Faraday Cage (pF)	Array2 Faraday Cage (pF)	Isolation (pF)	Silicon Wafer (pF)
Array1 Signal	3.67	$1.59x10^{-5}$	$1.09x10^{-3}$	$5.74x10^{-4}$
Array1 Ground	$9.44x10^{-3}$	$8.76x10^{-5}$	$4.48x10^{-3}$	$1.10x10^{-3}$
Array2 Signal	$1.57x10^{-5}$	3.67	$1.08x10^{-3}$	$5.70x10^{-4}$
Array2 Ground	$8.79x10^{-5}$	$9.47x10^{-3}$	$4.48x10^{-3}$	$1.10x10^{-3}$
Array1 Faraday Cage		$8.61x10^{-5}$	$1.07x10^{-2}$	3.66
Array2 Faraday Cage	$8.61x10^{-5}$		$1.07x10^{-2}$	3.66
Isolation	$1.07x10^{-2}$	$1.07x10^{-2}$		1.23
Silicon Wafer	3.66	3.66	1.23	

As the linearity of capacitance matrix was observed with the increasing row number it can be concluded that, for a high row number value, the capacitive behavior of regular and Faraday cage CMUT arrays can be compared regardless of the row number. For this purpose, the capacitance matrixes of the arrays with a high row number value were extrapolated as given in Tables 4.11 and 4.12, respectively.

Table 4.11. Extrapolated capacitance matrix of the regular CMUT array with a high row number value (N).

Node Names	Array1 Signal (xN pF)	Array1 Ground (xN pF)	Array2 Signal (xN pF)	Array2 Ground (xN pF)	Isolation (xN pF)	Silicon Wafer (xN pF)
Array1 Signal		$2.61x10^{-1}$	$2.51x10^{-8}$	$2.03x10^{-7}$	$6.97x10^{-5}$	$3.26x10^{-1}$
Array1 Ground	$2.61x10^{-1}$		$2.04x10^{-7}$	$1.60x10^{-6}$	$4.16x10^{-4}$	$8.54x10^{-4}$
Array2 Signal	$2.51x10^{-8}$	$2.04x10^{-7}$		$2.61x10^{-1}$	$6.93x10^{-5}$	$3.26x10^{-1}$
Array2 Ground	$2.03x10^{-7}$	$1.60x10^{-6}$	$2.61x10^{-1}$		$4.17x10^{-4}$	$8.57x10^{-4}$
Isolation	$6.97x10^{-5}$	$4.16x10^{-4}$	$6.93x10^{-5}$	$4.17x10^{-4}$		$8.83x10^{-2}$
Silicon Wafer	$3.26x10^{-1}$	$8.54x10^{-4}$	$3.26x10^{-1}$	$8.57x10^{-4}$	$8.83x10^{-2}$	

Table 4.12. Extrapolated capacitance matrix of the Faraday caged CMUT array with a high row number value (N).

Node Names	Array1 Signal (xN pF)	Array1 Ground (xN pF)	Array2 Signal (xN pF)	Array2 Ground (xN pF)
Array1 Signal		$2.61x10^{-1}$	$2.58x10^{-7}$	$1.43x10^{-6}$
Array1 Ground	$2.61x10^{-1}$		$1.41x10^{-6}$	$7.97x10^{-6}$
Array2 Signal	$2.58x10^{-7}$	$1.41x10^{-6}$		$2.61x10^{-1}$
Array2 Ground	$1.43x10^{-6}$	$7.97x10^{-6}$	$2.61x10^{-1}$	
Array1 Faraday Cage	$3.26x10^{-1}$	$7.29x10^{-4}$	$1.39x10^{-6}$	$7.79x10^{-6}$
Array2 Faraday Cage	$1.40x10^{-6}$	$7.75x10^{-6}$	$3.26x10^{-1}$	$7.32x10^{-4}$
Isolation	8.36x10-5	3.43x10-4	$8.29x10^{-5}$	$3.43x10_{-4}$
Silicon Wafer	$4.40x10^{-5}$	$8.32x10^{-5}$	$4.36x10^{-5}$	$8.35x10^{-5}$

Table 4.12. (Continued)

Node Names	Array1 Faraday Cage (xN pF)	Array2 Faraday Cage (xN pF)	Isolation (xN pF)	Silicon Wafer (xN pF)
Array1 Signal	$3.26x10^{-1}$	$1.40x10^{-6}$	$8.36x10^{-5}$	$4.40x10^{-5}$
Array1 Ground	$7.29x10^{-4}$	$7.75x10^{-6}$	$3.43x10^{-4}$	$8.32x10^{-5}$
Array2 Signal	$1.39x10^{-6}$	$3.26x10^{-1}$	$8.29x10^{-5}$	$4.36x10^{-5}$
Array2 Ground	$7.79x10^{-6}$	$7.32x10^{-4}$	$3.43x10^{-4}$	$8.35x10^{-5}$
Array1 Faraday Cage		$7.59x10^{-6}$	$8.13x10^{-4}$	$3.23x10^{-1}$
Array2 Faraday Cage	$7.59x10^{-6}$		8.14x10-4	3.23x10-1
Isolation	$8.13x10_{-4}$	$8.14x10^{-4}$		$8.76x10^{-2}$
Silicon Wafer	$3.23x10^{-1}$	$3.23x10^{-1}$	$8.76x10^{-2}$	

As there are 6 nodes in 2-element regular CMUT array, there are 15 capacitances in total. So that, the capacitance circuitry for 2-element regular CMUT array can be constructed as shown in Figure 4.5 where a capacitance between any node “X” and node “Y” is notated as “C_X_Y”, “X” and “Y” being the short notation of the node.

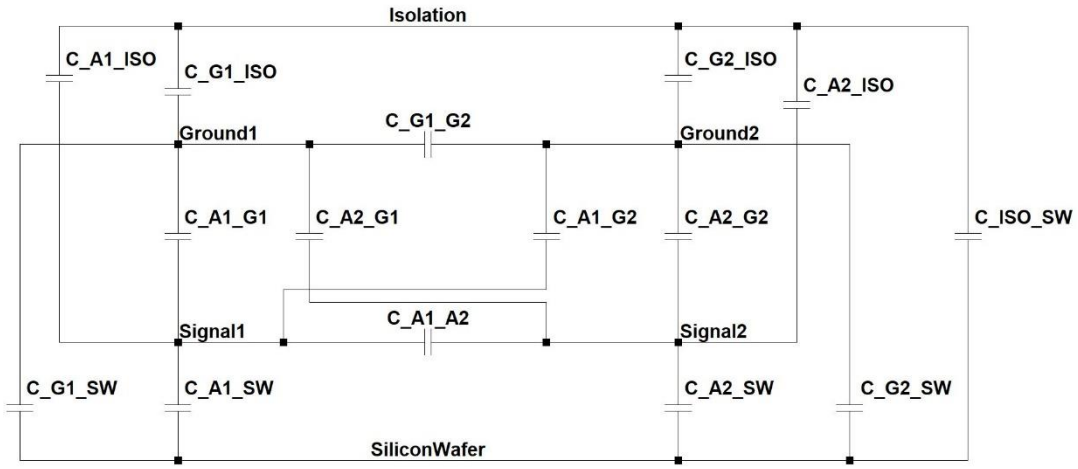


Figure 4.5. Representative capacitive circuitry schematic for 2-element regular CMUT array.

From the capacitance matrixes of regular CMUT array, it is observed that some capacitances are infinitesimal compared to others. For the ease of the theoretical calculations, capacitances with a value 100 times smaller than the most significant capacitance on that capacitance matrixes were treated as an open circuit. Furthermore, in the regular CMUT array operation, the isolation line, the top electrode of the first and second array elements, and the substrate are grounded. Based on the above information, the representative capacitive circuity of the regular CMUT array can be simplified to the circuitry given in Figure 4.6.

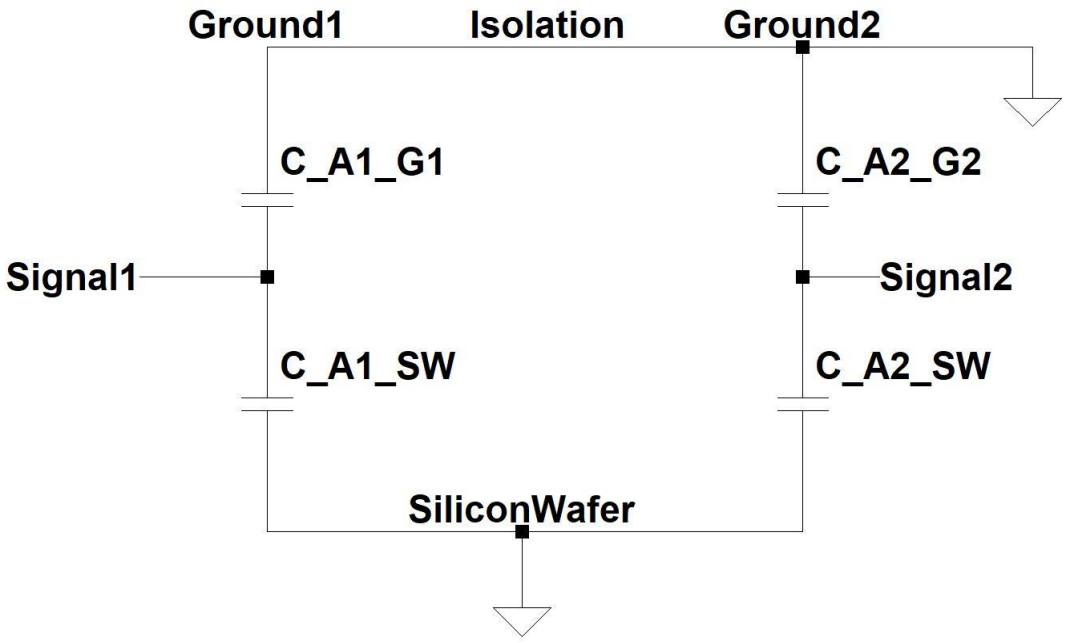


Figure 4.6. Simplified representative capacitive circuitry schematic for 2-element regular CMUT array.

For the theoretical calculation of the total array to ground capacitance (C_{Tot}), the parasitic capacitance (C_{Par}) and the coupling capacitance ($C_{Coupling}$) of the regular CMUT array, equations 4.1-4.3 were used.

$$C_{Tot} = C_{A1\_G1} + C_{A1\_SW} \tag{4.1}$$

$$C_{Par} = C_{TOT} - C_{A1\_G1} = C_{A1\_SW} \tag{4.2}$$

$$C_{Coupling} = \left(C_{A1\_G1} + C_{A1\_SW}\right)/2 \tag{4.3}$$

As there is 8 nodes in 2-element Faraday caged CMUT array, there are 28 capacitance in total. So that, the capacitance circuitry for 2-element Faraday caged CMUT array can be constructed as shown in Figure 4.7 where a capacitance between any node "X" and node "Y" is notated as "C_X_Y", "X" and "Y" being the short notation of the node.

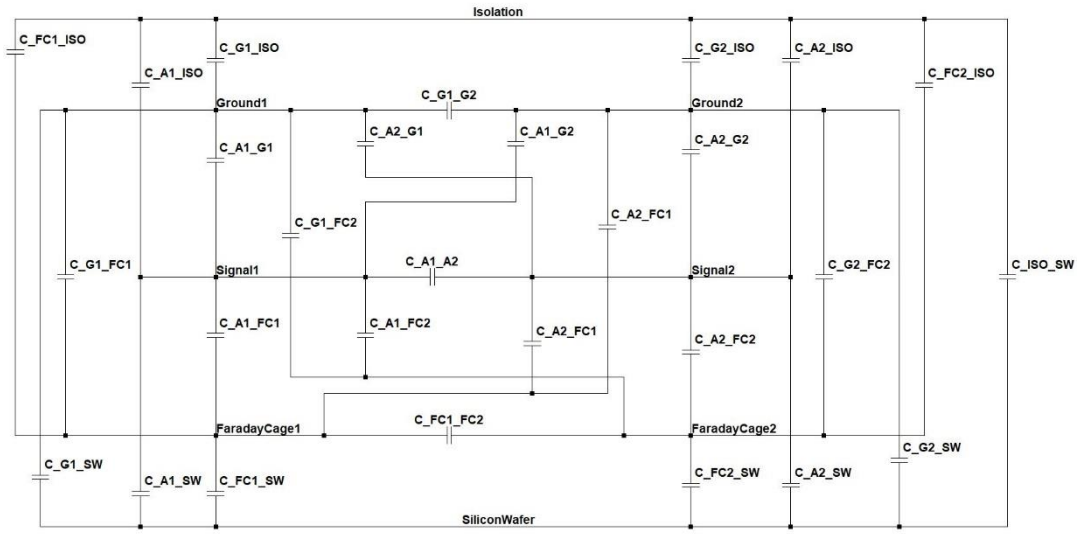


Figure 4.7. Representative capacitive circuitry schematic for 2-element Faraday caged CMUT array.

From the capacitance matrixes of Faraday caged CMUT array, it is observed that some capacitances are infinitesimal compared to others. For the ease of the theoretical calculations, capacitances with a value 100 times smaller than the most significant capacitance on that capacitance matrixes were treated as an open circuit. Furthermore, in the Faraday caged CMUT array operation, the isolation line, the top electrode of the first and second array element, and the substrate are grounded whereas the Faraday cage of the first array element and the Faraday cage of the second array element can be floating or grounded. Based on the above information, the simpler version of representative capacitance circuitry of Faraday caged CMUT array is depicted in Figure 4.8.

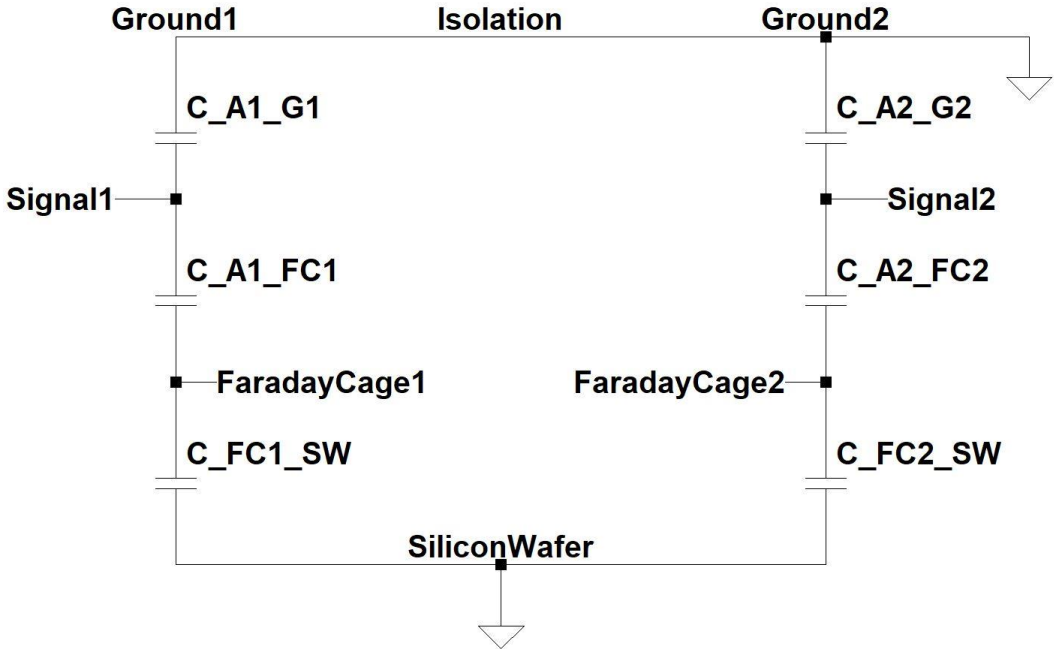


Figure 4.8. Simplified representative capacitive circuitry schematic for 2-element Faraday caged CMUT array.

For the theoretical calculation of the total array to ground capacitance (C_{Tot}), the parasitic capacitance (C_{Par}), and the coupling capacitance ($C_{Coupling}$) during the grounded operation the Faraday Cages of the 2-element Faraday caged CMUT array, the equations 4.4-4.6 were used.

$$C_{Tot} = C_{A1\_G1} + C_{A1\_FC1} \tag{4.4}$$

$$C_{Par} = C_{TOT} - C_{A1\_G1} = C_{A1\_FC1} \tag{4.5}$$

$$C_{Coupling} = \left(C_{A1\_G1} + C_{A1\_FC1}\right)/2 \tag{4.6}$$

For the theoretical calculation of the total array to ground capacitance (C_{Tot}), the parasitic capacitance (C_{Par}), and the coupling capacitance ($C_{Coupling}$) during the floating operation of the Faraday cages of the 2-element Faraday caged CMUT array, equations 4.7-4.9 were used. During the floating operation of Faraday Cages, since there is an additional series capacitance from bottom electrode to the substrate, it has been expected that the floating operation of the Faraday cages of the Faraday caged

CMUT array would supress the capacitive effects on the bottom electrode coming through the substrate compared to the regular CMUT array.

$$C_{Tot} = C_{A1\_G1} + (C_{A1\_FC1} // C_{FC1\_SW}) \quad (4.7)$$

$$C_{Par} = C_{TOT} - C_{A1\_G1} = (C_{A1\_FC1} // C_{FC1\_SW}) \quad (4.8)$$

$$C_{Coupling} = \left(C_{A1\_G1} + (C_{A1\_FC1} // C_{FC1\_SW})\right)/ 2 \quad (4.9)$$

ADS can be used as a circuit simulator to calculate the total array to ground and coupling capacitances. From the total array to ground capacitance, the parasitic capacitance through the substrate can also be calculated. Based on the extracted or extrapolated capacitance matrixes from the Semulator3D simulations, the capacitance circuitries of regular and Faraday caged CMUT arrays were constructed in ADS using the capacitive circuitry schematics given in Figure 4.5 and Figure 4.7 as the template, respectively.

In ADS, two different configurations were used to examine the capacitive behavior of the capacitance circuitries. For the total array to ground capacitance calculation, the pin of "Array 1 Signal" was connected to signal source with 50 Ohm input resistance whereas the pin of "Array 2 Signal" was floating.

CMUTs have high electrical input impedance compared to other ultrasonic transducers, which results in reduced sensitivity [73,74]. Routing the receive path through high input impedance preamplifiers employing resistive feedback is the common way to shunt the parasitic capacitance. This is an additional method to reduce parasitic capacitance from the outside of the CMUT array, whereas in this study the intrinsic parasitic capacitance of CMUT arrays were investigated and compared. Therefore, the effect of the receive circuitry on the parasitic capacitance was not included in the content of the study.

For the coupling capacitance calculation, a signal source with 50 Ohm input resistance is connected between the pins of "Array 1 Signal" and "Array 2 Signal". For both of the configurations the capacitance seen by the signal source is calculated through the equation set given in the Eq. 4.10- 4.13. The simulations were performed

from 1MHz to 10 MHz, which is a reasonable range for CMUT array characterization. As it was expected the capacitance values were constant over the frequency range, therefore the mean values were used as the numerical result. For the extraction of the capacitance seen by the signal source the following equation set (Eq. 4.10-4.13) was used.

$$Z_{Complex} = Z_{in}(S_{11}) \tag{4.10}$$

$$R = Real(Z_{Complex}) \tag{4.11}$$

$$I = Imag(Z_{Complex}) \tag{4.12}$$

$$C = abs\left(\frac{1}{I \times 2\pi f}\right) \tag{4.13}$$

In addition to capacitive circuit simulations, ADS was used for construction and FEM modeling of 3-D structure of the regular and Faraday caged CMUT arrays. For the construction of the regular and Faraday caged CMUT arrays, substrate technologies were defined. In ADS, substrate technologies are defined layer by layer where each layer has a determined thickness. In a substrate technology, it is possible to construct a via inside a layer that has the same thickness with the layer and has an assigned material and layout mask code. In addition, between layers it is possible to define 2-D structures that have an assigned material and layout mask code. In accordance with the explained abilities of ADS for defining a substrate technology, substrate technologies for regular and Faraday caged CMUT arrays were defined based on the representative structures given in Figure 4.3 and given thickness parameter in Table 4.1. Moreover, according to the defined substrate technology, layout designs for regular and Faraday caged CMUT arrays with row number values of 1,2,3 and 10 were realized with the parameters given in Table 4.1. In Figure 4.9, the constructed structures of regular and Faraday caged CMUT arrays with a row number of value 10 in ADS are given.

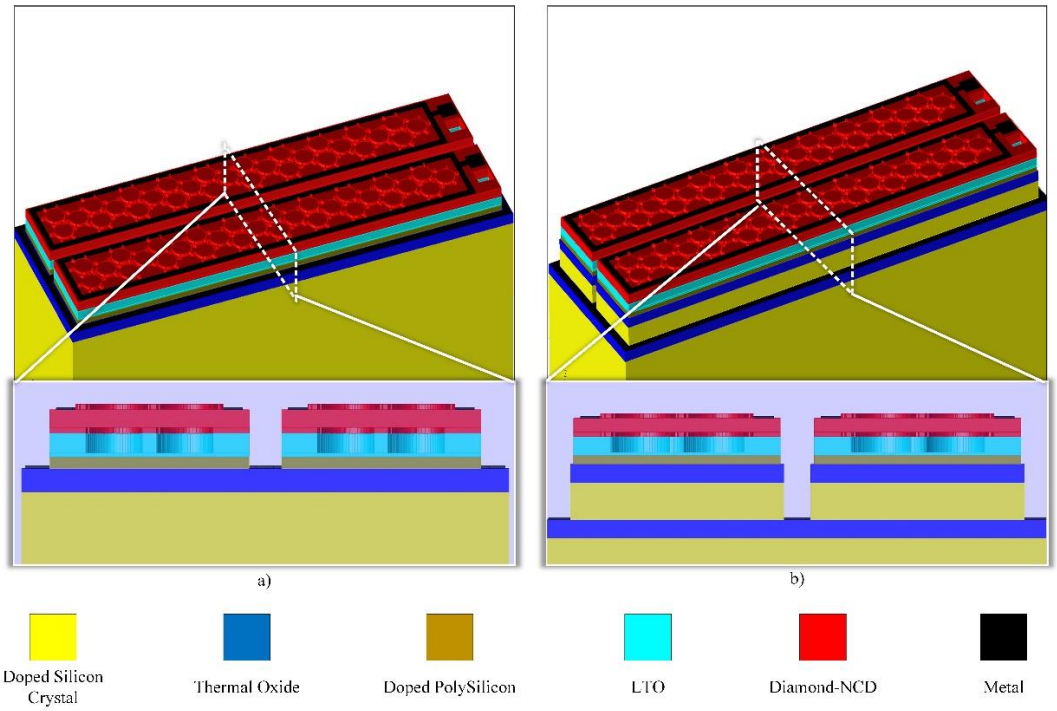


Figure 4.9. The constructed structures of regular (a) and Faraday caged (b) CMUT arrays with a row number value of 10 in ADS.

EMPro provided the Electro-magnetic (EM) solutions of the FEM modeled 3-D structures, working coherently with ADS. After EM simulations of the structures were done, the EM solutions performed by EMPro were automatically imported into ADS so that, with the construction of the required configurations in ADS, the capacitive behavior of the regular and Faraday Cages CMUT arrays were found out. The configurations constructed for extracting the capacitive behavior (total array to ground and coupling capacitance) of the capacitance circuitries described above were also constructed for the capacitive behavior analysis of the 3-D built structures in ADS.

Due to the computational complexity, it is not feasible to construct a 3-D regular and Faraday caged CMUT array with a very high row number. Therefore, the EM solutions of the regular and Faraday caged CMUT arrays with a very high row number value (N) were not provided. Therefore, the capacitive behavior of the

regular and Faraday caged CMUT arrays with a very high row number inferred by the EM solutions were not investigated nor presented.

The total array to ground (C_{Tot}) and the parasitic capacitance (C_{Par}) found through theoretical calculations, circuit simulator, and EM solution of the 3-D built structure of the regular CMUT array are as given in Table 4.13. The coupling capacitance ($C_{Coupling}$) found through theoretical calculations, circuit simulator, and EM solution of 3-D built structure of the regular CMUT array are as given in Table 4.14. It is observed that the capacitive behavior of the regular CMUT array, found through the different sources (theory, circuit simulation and EM simulation) are in agreement with each other. Thus, it is concluded that the capacitive feature of the capacitance circuitry for a high row number case can represent the capacitive feature of the regular CMUT array regardless of the row number.

Table 4.13. The total array to ground (C_{Tot}) and parasitic capacitance (C_{Par}) of the regular CMUT array calculated through several evaluation types.

Result Type		**Theoretical Result (pF)**	**Circuit Simulation (pF)**	**EM Simulation (pF)**
Row # 1	C_{Tot}	1.43	1.43	1.43
	C_{Par}	0.75	0.75	0.74
Row # 2	C_{Tot}	2.01	2.01	2.01
	C_{Par}	1.07	1.07	1.06
Row # 3	C_{Tot}	2.60	2.61	2.64
	C_{Par}	1.40	1.40	1.42
Row # 10	C_{Tot}	6.70	6.71	6.77
	C_{Par}	3.67	3.68	3.72
Row # N (x N)	C_{Tot}	0.59	0.59	-
	C_{Par}	0.33	0.33	-

Table 4.14. The coupling capacitance ($C_{Coupling}$) of the regular CMUT array calculated through several evaluation types.

Result Type	Theoretical Result (pF)	Circuit Simulation (pF)	EM Simulation (pF)
Row # 1	0.71	0.71	0.72
Row # 2	1.01	1.01	1.00
Row # 3	1.30	1.31	1.31
Row # 10	3.35	3.36	3.39
Row # N (× N)	0.29	0.29	-

The total array to ground (C_{Tot}) and the parasitic capacitance (C_{Par}) found through theoretical calculations, circuit simulator, and EM solution of 3-D built structure of the Faraday caged CMUT array during the grounded operation of the Faraday cages are as given in Table 4.15. The coupling capacitance ($C_{Coupling}$) found through theoretical calculations, circuit simulator, and EM solution of 3-D built structure of the Faraday caged CMUT array during the grounded operation of the Faraday cages are as given in Table 4.16. It is observed that the capacitive behavior of the Faraday caged CMUT array for the grounded operation of the Faraday cages, found through different sources (theory, circuit simulation and EM simulation) are in agreement with each other. Thus, it is concluded that the capacitive feature of the capacitance circuitry for a high row number case can represent the capacitive feature during the grounded operation of the Faraday cages of the Faraday caged CMUT array regardless of the row number.

Table 4.15. The total array to ground (C_{Tot}) and parasitic capacitance (C_{Par}) of the Faraday caged CMUT array during the grounded operation of the Faraday Cages calculated through several evaluation types.

Result Type		**Theoretical Result (pF)**	**Circuit Simulation (pF)**	**EM Simulation (pF)**
Row # 1	C_{Tot}	1.43	1.43	1.40
	C_{Par}	0.75	0.75	0.71
Row # 2	C_{Tot}	2.01	2.01	2.01
	C_{Par}	1.07	1.07	1.06
Row # 3	C_{Tot}	2.61	2.60	2.56
	C_{Par}	1.40	1.35	1.34
Row # 10	C_{Tot}	6.70	6.70	6.61
	C_{Par}	3.67	3.67	3.56
Row # N (x N)	C_{Tot}	0.59	0.59	-
	C_{Par}	0.33	0.33	-

Table 4.16. The coupling capacitance ($C_{Coupling}$) of the Faraday Caged CMUT array during the grounded operation of the Faraday cages calculated through several evaluation types.

Result Type	**Theoretical Result (pF)**	**Circuit Simulation (pF)**	**EM Simulation (pF)**
Row # 1	0.71	0.71	0.72
Row # 2	1.01	1.01	1.00
Row # 3	1.30	1.31	1.31
Row # 10	3.35	3.36	3.39
Row # N (× N)	0.29	0.29	-

The total array to ground (C_{Tot}) and parasitic capacitance (C_{Par}) found through theoretical calculations, circuit simulator, and EM solution of 3-D built structure of the Faraday caged CMUT array during the floating operation of the Faraday cages are as given in Table 4.17. The coupling capacitance ($C_{Coupling}$) found through

theoretical calculations, circuit simulator, and EM solution of 3-D built structure of the Faraday caged CMUT array during the floating operation of the Faraday cages are as given in Table 4.18. It is observed that the capacitive behavior of the Faraday caged CMUT array for the grounded operation of the Faraday cages, found through different sources (theory, circuit simulation and EM simulation) are in agreement with each other. Thus, it is concluded that the capacitive feature of the capacitance circuitry for a high row number case can represent the capacitive feature during the grounded operation of the Faraday cages of the Faraday caged CMUT array regardless of the row number.

Table 4.17. The total array to ground (C_{Tot}) and parasitic capacitance (C_{Par}) of the Faraday caged CMUT array during the floating operation of the Faraday cages calculated through several evaluation types.

Result Type		**Theoretical Result (pF)**	**Circuit Simulation (pF)**	**EM Simulation (pF)**
Row # 1	C_{Tot}	1.06	1.06	1.04
	C_{Par}	0.38	0.38	0.35
Row # 2	C_{Tot}	1.48	1.48	1.48
	C_{Par}	0.54	0.54	0.53
Row # 3	C_{Tot}	1.91	1.90	1.90
	C_{Par}	0.71	0.70	0.68
Row # 10	C_{Tot}	4.86	4.87	4.88
	C_{Par}	1.83	1.84	1.83
Row # N (x N)	C_{Tot}	0.42	0.42	-
	C_{Par}	0.16	0.16	-

Table 4.18. The coupling capacitance ($C_{Coupling}$) of the Faraday caged CMUT array during the floating operation of the Faraday cages calculated through several evaluation types.

Result Type	**Theoretical Result (pF)**	**Circuit Simulation (pF)**	**EM Simulation (pF)**
Row # 1	0.53	0.53	0.52
Row # 2	0.74	0.74	0.74
Row # 3	0.96	0.95	0.95
Row # 10	2.43	2.44	2.44
Row # N (× N)	0.21	0.21	-

Based on the calculated results given in Tables 4.13-4.18, in Table 4.19 the parasitic capacitance (C_{Par}) and coupling capacitance ($C_{Coupling}$) of regular and Faraday caged CMUT arrays with a very high row number (N) are given to compare the capacitive behavior of the arrays.

Table 4.19. The parasitic capacitance (C_{Par}) and coupling capacitance ($C_{Coupling}$) of regular and Faraday caged CMUT arrays with a very high row number (N).

Array Type		**Row # N (x N pF)**
Regular CMUT Array	C_{Par}	0.33
	$C_{Coupling}$	0.29
Faraday Caged CMUT Array Grounded Faraday Cages	C_{Par}	0.33
	$C_{Coupling}$	0.29
Faraday Caged CMUT Array Floating Faraday Cages	C_{Par}	0.16
	$C_{Coupling}$	0.21

Based on the calculated theoretical and simulations results, the parasitic capacitance (C_{Par}) and the coupling capacitance ($C_{Coupling}$) of the Faraday caged CMUT array for grounded and floating operation of the Faraday cages were compared with the capacitive behavior of regular CMUT array. The comparison was performed between the corresponding substrate types of the CMUT arrays. It is observed that, floating operation of Faraday cages of the Faraday caged CMUT array offers

51.5 % less parasitic capacitance compared to both grounded operation of the Faraday cages of the Faraday caged CMUT array and regular CMUT array.

Coupling coefficient is an important figure of merit of a transducer since it is the ratio delivered to mechanical energy to total stored energy. The relation of the coupling coefficient (k_T^2) and the parasitic capacitance (C_{Par}) as given in the Eq. 4.14 [75].

$$k_T{}^2 = \frac{V\frac{dC}{dV}}{C_{Par}+V\frac{dC}{dV}} \tag{4.14}$$

where V is the applied biasing voltage and *dC/dV* term represents the change in the capacitance due to vibration of the membrane. Therefore, reduction of parasitic capacitance improves the energy conversion efficiency of the transducer.

Furthermore, the floating operation of Faraday cages of the Faraday caged CMUT array offers 27.6 % less coupling capacitance compared to both grounded operation of the Faraday cages of the Faraday caged CMUT array and regular CMUT array.

In addition to the extracting the capacitive behavior of the 3-D built structures, the electrical crosstalk between neighboring elements were also found out through the provided EM solutions of the structures as depicted in Figure 4.11. For electrical crosstalk analysis, the pin of the “Array1 Signal” was connected to a signal source with 50 Ohm input resistance, whereas the pin of the “Array2 Signal” was connected to another signal source with 50 Ohm input resistance.

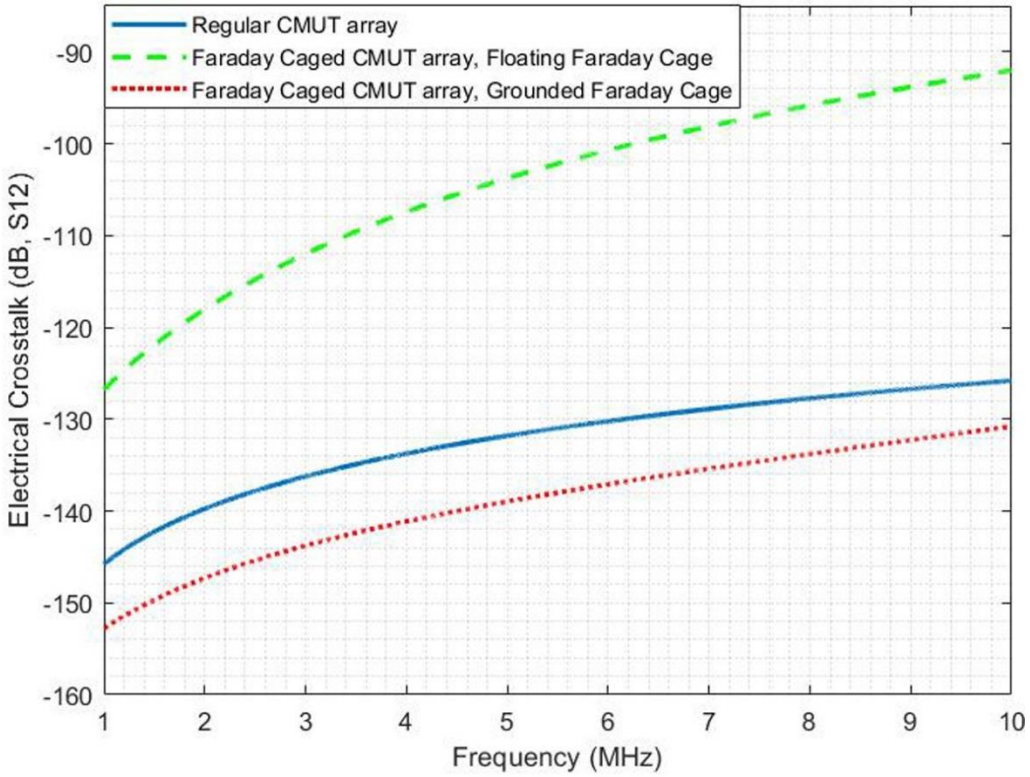


Figure 4.10. Electrical crosstalk of the regular and Faraday caged CMUT array with row number value of 10.

On the constructed configuration, the S_{12} parameter was observed over the frequency range of 1 MHz to 10 MHz to find out the electrical crosstalk. Instead, EM solutions of the regular and Faraday caged CMUT arrays with row number of 10 (as a high row number approximation) were used to compare the electrical crosstalk behavior of the arrays.

As seen from Figure 4.10, the electrical crosstalk increased with frequency. The minimum, mean and maximum crosstalk value of the 3-D built structures of the regular and Faraday caged CMUT array for floating and grounded operation when the row number is 10 are as given in Table 4.20.

Table 4.20. The electrical crosstalk feature of 3-D built structures of the regular CMUT array and Faraday caged CMUT array for floating and grounded operation of Faraday cages.

	Regular CMUT array	**Faraday caged CMUT array**	
Faraday Cage		**Floating**	**Grounded**
Electrical Crosstalk (Min at 1 MHz), dB	-145.8	-126.8	-152.8
Electrical Crosstalk (Max at 10 MHz), dB	-125.8	-92.0	-130.8
Electrical Crosstalk (Mean, 1-10 MHz), dB	-132.3	-104.3	-139.0

It is observed that the grounded operation of Faraday cages of the Faraday caged CMUT array offers 34.7 dB and 6.7 dB decrease in overall (mean value) over the frequency range of 1 MHz to 10 MHz compared to floating operation of Faraday cages of the Faraday caged CMUT array and regular CMUT array, respectively. The main difference between the electrical crosstalk behavior of regular CMUT array and the grounded Faraday cage operation of the Faraday caged CMUT array can be explained as the difference between the resistivity of Faraday cage and substrate. In simulations the substrate was grounded from the backside, has a resistivity of 5 Ω.cm and the thickness of the substrate was 400 μm whereas Faraday cage was grounded from the top surface, has a resistivity of 0.005 Ω.cm, and the thickness was 2 μm.

4.3 Proposed Transmit and Receive Operation

The active capacitance of a CMUT cell is the capacitance between the bottom electrode and the moveable region of the top electrode. However, the total capacitance between the bottom and the top electrodes is more than the active capacitance of the CMUT cell because of the parallel parasitic capacitance. As it was observed through the simulations there is an additional capacitance between the signal and ground electrode of the CMUT array element coming through the substrate. In the transmit operation, the parasitic capacitance is of little concern, however, the parasitic capacitance drastically reduces the receiving sensitivity and the coupling efficiency of a CMUT [76-78]. The coupling coefficient determines the bandwidth of the transducer and the effective use of the energy and therefore it is an important figure of merit of a transducer [75].

Crosstalk is the coupling of energy between the elements of a CMUT array. The electrical crosstalk is the crosstalk mechanism caused by the coupling of the electromagnetic wave from one array element to another [78]. Since the applied voltage is much higher in transmit operation compared to the detected voltage in receiving operation, the electrical crosstalk is much more effective in transmit operation of the CMUT array. The electrical crosstalk increases the noise in the system, and it degrades the focusing and imaging performance.

From the FEA simulations of the regular and Faraday caged CMUT arrays the followings were concluded [79].

- Compared to the regular CMUT array in the Faraday caged CMUT array, for floating operation of Faraday cage, the parasitic capacitance decreased by 51.5 %.
- Compared to the regular CMUT array in the Faraday caged CMUT array, for floating operation of Faraday cage, the coupling capacitance decreased by 27.6 %.

- Compared to the regular CMUT array in the Faraday caged CMUT array, for grounded operation of Faraday cage, the electrical crosstalk decreased by 6.7 dB.

From these facts stated above, it is observed that, during the receive operation, the floating operation of the Faraday cage is advantageous in terms of improving the receiving sensitivity and coupling coefficient since it offers reduction in parasitic capacitance, whereas during the transmit operation the grounded operation of Faraday cage is beneficial in terms of reducing the noise in the system since the electrical crosstalk is declined.

In addition to the Faraday caged CMUT array an accompanying transmit and receive operation for Faraday cage is proposed in which, while the CMUT array element is in transmit (TR) mode, the switch, which is connecting the Faraday cage to the ground, is closed, and thus, the Faraday cage is in grounded (GND) state, whereas while the array element is in receive (RX) mode, the switch, is open, and thus, the Faraday cage is in floating (FLT) state [79]. Figure 4.11 shows the proposed operational method for the Faraday caged CMUT array.

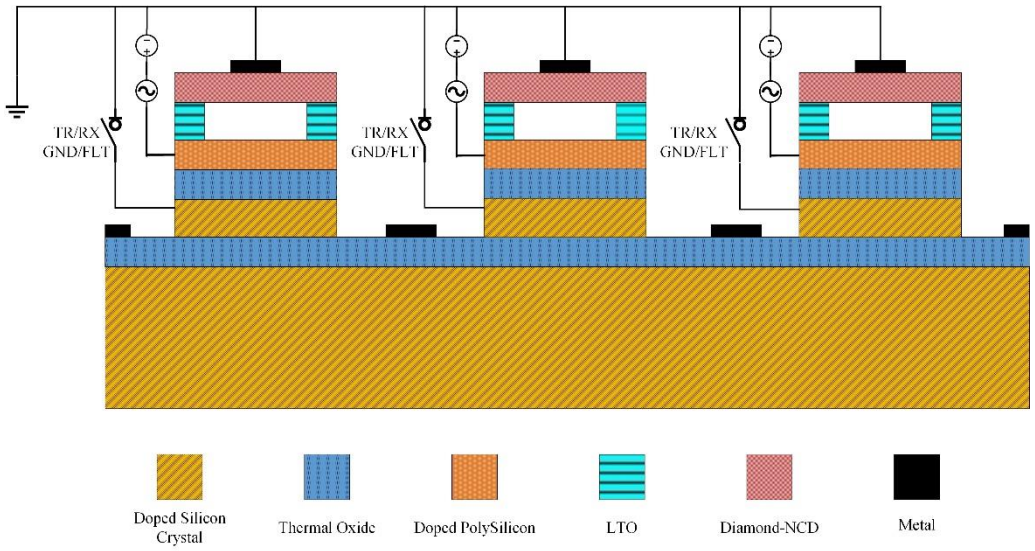


Figure 4.11. The proposed operational method for the Faraday caged CMUT array.

Therefore, with the proposed operation regime for Faraday cages, during the receive operation of CMUT array element, Faraday cage is in floating state so that the parasitic capacitance is decreased by 51.5 % and the coupling capacitance is decreased by 27.6 % resulting in improved receive sensitivity and coupling coefficient; whereas during the transmit operation, Faraday cage is in grounded state so that the electrical crosstalk is decreased by 6.7 dB resulting in less noise in the system [79].

CHAPTER 5

CONCLUSION

The microfabrication process flow for diamond membrane CMUT array based on the sacrificial etching of polysilicon in XeF_2 plasma to realize diamond membrane CMUT array having a large number of array elements is developed and presented. The microfabrication requires 6 lithography masks. The stiction problem of the membranes in wet etching processes is also avoided since XeF_2 is gaseous etchant and provides dry release.

Based on the developed microfabrication process flow, two identical 64-element 1-D CMUT arrays were designed so that in the collapse-snapback mode, it would operate as a HIFU array at 2 MHz, whereas in the collapse mode, it would operate as a FAST array at 8 MHz for transmitting and receiving ultrasound waves at high speed. Therefore, CMUT arrays were designed to have a resonance frequency of between 3 MHz and 4 MHz in the conventional mode underwater. The collapse voltage of the designed CMUT arrays was calculated as 70 V.

In addition to the proposed microfabrication, a CMUT array structure named Faraday caged CMUT and a transmit and receive operation are proposed for electrical crosstalk and parasitic capacitance reduction.

The proposed Faraday caged CMUT includes an individual third electrode for each CMUT array element placed under the bottom electrode that acts as a Faraday cage and electrically controlled by the third terminal of the array element. Based on the results from the FEM simulations, it is observed that it is advantageous to operate the Faraday cage of an array element as grounded and floating during the transmitting and receiving operations of the array element, respectively.

According to the FEM simulations, during the receive operation of the array element the proposed Faraday Caged CMUT array and the accompanying transmit and

receive operation of Faraday cage offer 51.5 % less parasitic capacitance and 27.6 % less coupling capacitance resulting enhanced receive sensitivity and coupling coefficient; whereas during the transmit operation of the array element a 6.7 dB decrease in electrical crosstalk is offered resulting less noise in the system.

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